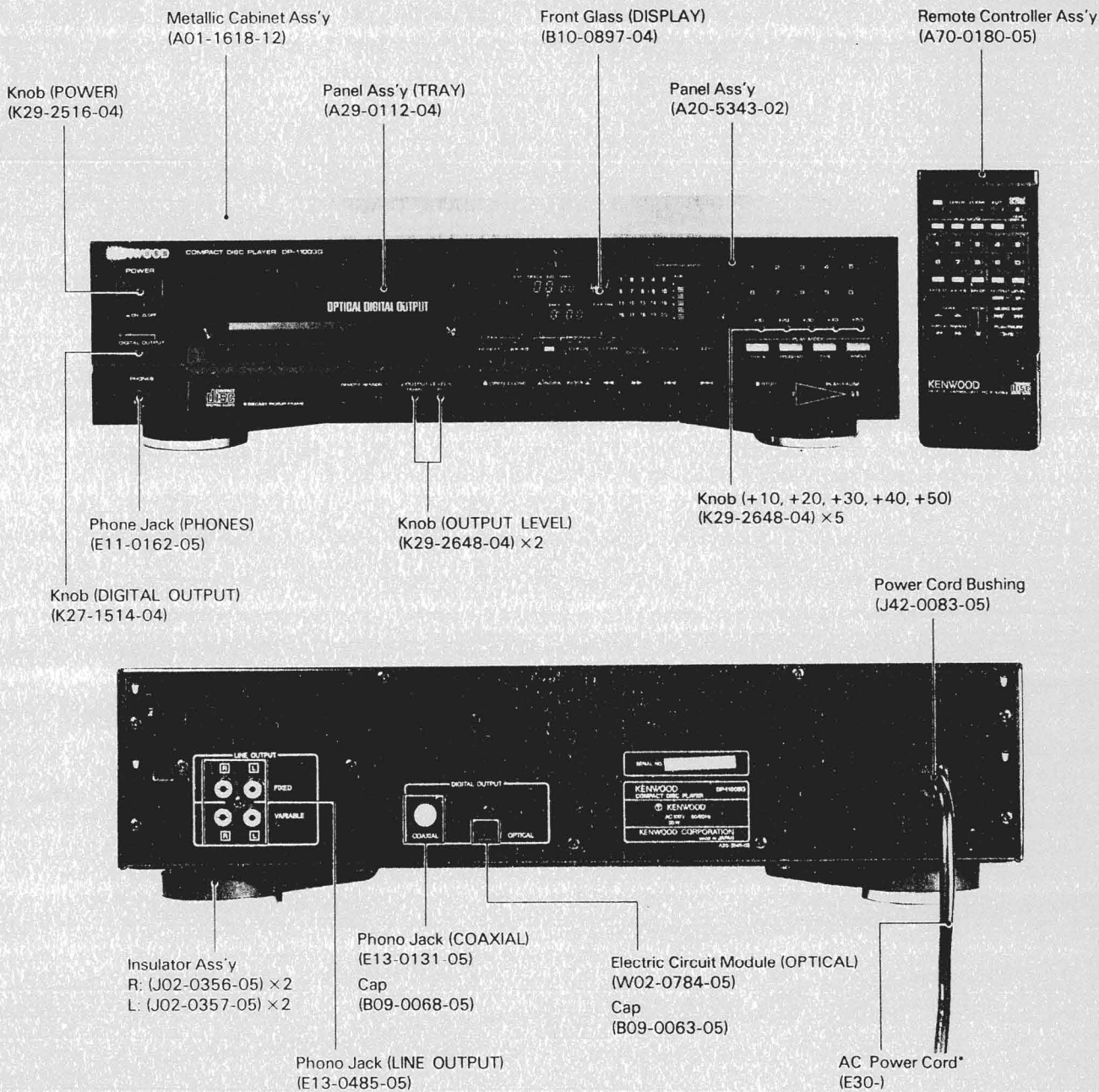


DP-1100SG

SERVICE MANUAL

©1988-1 PRINTED IN JAPAN
B51-3358-00(B)1312



In compliance with Federal Regulations, following are reproductions of labels on, or inside the product relating to laser product safety.

KENWOOD-Corp. certifies this equipment conforms to DHHS Regulations No. 21 CFR 1040.10, Chapter 1, Subchapter J.

DANGER: Laser radiation when open and interlock defeated.
AVOID DIRECT EXPOSURE TO BEAM.

* Refer to parts list on page 85.

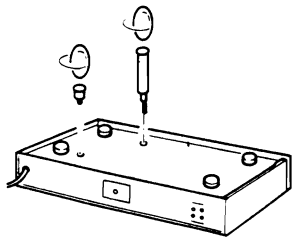
CONTENTS

TRANSPORTATION SCREW 2
 DISASSEMBLY FOR REPAIR 3
 SYSTEM CONNECTIONS 4
 CONTROLS AND INDICATORS 5
 BLOCK DIAGRAM 7
 CIRCUIT DESCRIPTION 9
 • Description of components 9
 • Set Mode Flowchart 11
 • Test mode 12
 • Microprocessor
 μPD75216ACV-051 (X32-1170-00: IC10) 17
 • RF amplifier
 CXA1081M (X29-1870-00: IC1) 20
 • Servo signal processor
 CXA1244S (X32-1170-00: IC1) 26
 • Digital signal processing LSI
 CXD1125QZ (X32-1170-00: IC6) 30
 • Static RAM
 CXK5816SP-12L (X32-1170-00: IC7) 51
 • Reset IC
 M51951ASL (X32-1170-00: IC11) 52

• DA Converter
 PCM56P-K (X25-3050-00: IC1, IC2) 53
 • Digital filter
 SM5804D (X25-3050-00: IC14) 54
 • D/A distortion correct
 TC17G005AF-0048 (X25-3050-00: IC15) 58
 • Hexa D Flip-flop
 TC74HC174F (X25-3040-00: IC2) 58
 • Transistor array
 TD62003AP (X25-3040-00: IC3) 59
 • 2-channel analog switch IC
 μPD4053BC (X32-1170-00: IC2) 59
 ADJUSTMENT/REGLAGE/ABGLEICH 60
 PC BOARD (Component Side View) 67
 PC BOARD (Foil Side View) 71
 SCHEMATIC DIAGRAM 75
 EXPLODED VIEW (MECHANISM) 83
 EXPLODED VIEW (UNIT) 84
 PARTS LIST 85
 SPECIFICATIONS Back cover

Transportation screw

Before operation, remove the two red screws attached to the bottom of the unit used during transport from the factory. Remove both screws using a coin, etc. and, after removing, retain them together with the Warranty card and other documents. When the unit is to be transported again, be sure to replace the two screws to their original position:



■ Before transport: tighten the transportation screws

Before transporting this unit, be sure to tighten the two transportation screws on the bottom of the unit.

1. Turn ON the power switch when no disc is loaded.
2. Wait a few seconds until the disc OUT indicator comes "ON". Then turn "OFF" the power.

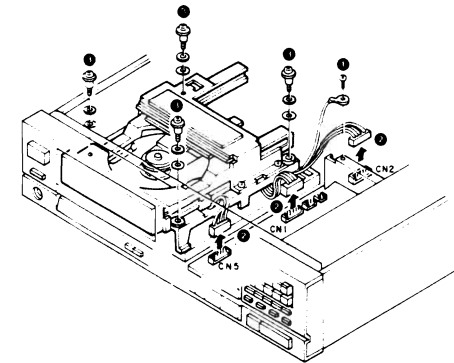


3. Firmly tighten the two transportation screws.

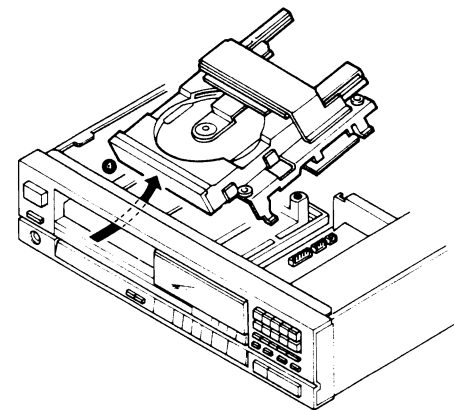
DISASSEMBLY FOR REPAIR

Mechanism assembly removal procedure

1. Remove the screw (1) retaining the ground lug from the mechanism assembly.
2. Remove the three connectors (2).
3. Remove the four screws (3) retaining the mechanism assembly.



4. Remove the mechanism assembly by pulling out in the direction of the arrow (4).

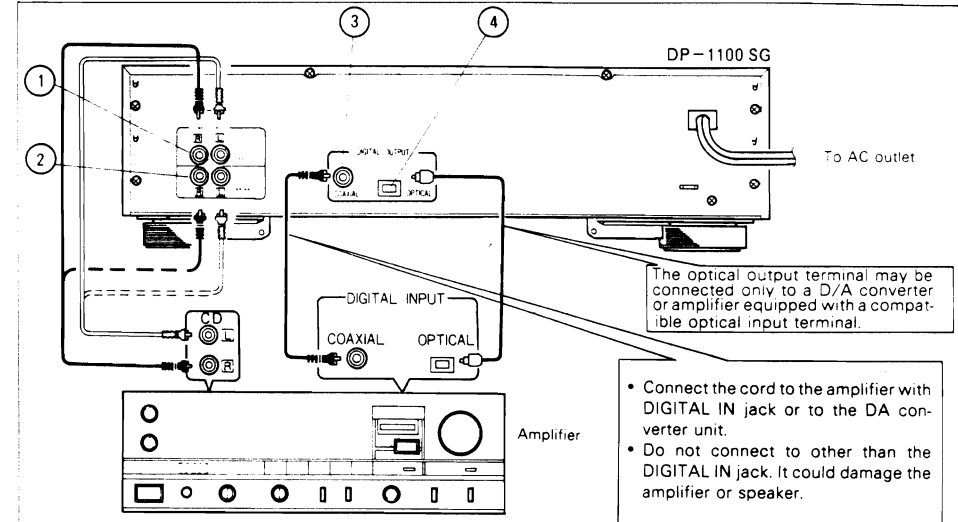


SYSTEM CONNECTIONS

Connection precautions

Always turn OFF the power before making connections.

Incorrect connections can cause damage to your audio system. Heed the precautions and follow the directions carefully.



① **Fixed output (FIXED): Output voltage 2Vrms fixed**
Use these stereo output jacks for connection to a typical amplifier or receiver.

② **Variable output (VARIABLE): Output voltage 0~2Vrms variable**
You can adjust the output level from these jacks to match the signal level of other sources connected to your amplifier or receiver. (May also be used for adjusting recording level by remote control).

③ **Digital output (DIGITAL OUT, COAXIAL) 0.5Vp-p 75 ohms**

④ **Optical output (DIGITAL OUT, OPTICAL) -15dBm ~ -25dBm**

Note:

1. If your amp has both optical and coax digital inputs, use only one or the other. Connection to both creates a loop which can cause undesirable oscillation.
2. Be careful never to kink, twist or bend the optical fiber cable excessively.
3. This unit is not necessarily compatible with the optical fiber cables provided by other manufacturers. If connection is not successful, consult your dealer or service representative.

■ **Connection to amplifier or receiver**
(The following three methods are possible.)

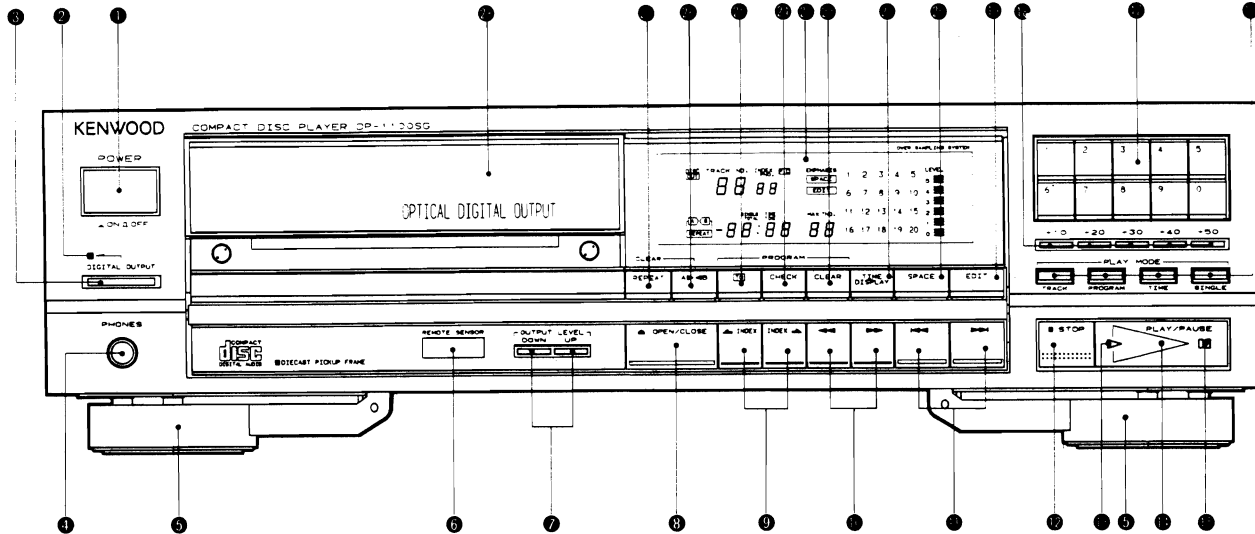
Plug in the AC power cord for the CD player and amplifier.

- **Conventional amplifier connection:**
Connect the CD player's LINE OUTPUT (FIXED or VARIABLE) to the AUX or CD input jacks on the rear panel of the amp or receiver. Use the supplied cord. Be sure to connect the left (L) and right (R) jacks on the CD player to the corresponding jacks on the amplifier or receiver.
- **Connection to an amplifier equipped with digital input:**
Use a single coaxial cable to connect the CD player's DIGITAL OUT jack to the digital input jack on the amplifier.
- **Connection to a component equipped with optical fiber cable (OPTICAL INPUT) terminal:**
Use an optical fiber cable to connect the CD player's (DIGITAL OUT) OPTICAL terminal to the optical input terminal on the other component.

DP-1100SG DP-1100SG

CONTROLS AND INDICATORS

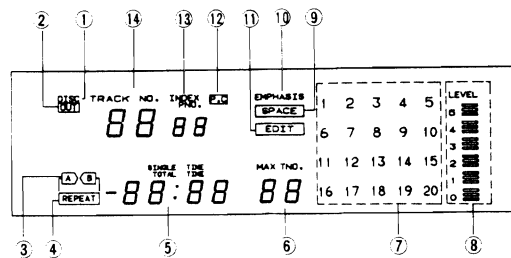
- ➊ **POWER switch**
- ➋ **DIGITAL OUTPUT indicator**
This illuminates when the digital output switch is on.
- ➌ **DIGITAL OUTPUT switch**
This switches digital output on and off.
- ➍ **PHONES jack**
Plug stereo headphones into this jack.
- ➎ **Dyna-pneumatic suspension**
Designed to safeguard sound quality by isolating the player from adverse external vibrations.
Note:
To maintain the effectiveness of the Dyna-pneumatic suspension, do not place other components or items weighing more than 5kg on top of this unit.
- ➏ **REMOTE SENSOR window**
This picks up infrared signals from the remote control.
- ➐ **OUTPUT LEVEL adjustment keys**
These DOWN/UP keys simultaneously adjust both the rear panel VARIABLE output signal level and headphone volume. The output level setting is shown by the indicators on the right side of the display.
- ➑ **OPEN/CLOSE key (▲)**
Press once to open the disc tray. Press again to close.
- ➒ **INDEX keys (◀ INDEX ▶)**
Used to specify index numbers within tracks.



- ➓ **Numeric keys (1 ~ 0)**
Used to specify first digit in a number when selecting a tune or setting a time.
- ➔ **Numeric keys (+10 ~ +50)**
Adds ten to a number. Used with the numeric keys.
- ➕ **EDIT key**
Used to automatically fit tracks into a program of a specified time length.
- ➗ **SPACE key**
This causes play to pause for about four seconds between tunes, useful when taping.
- ➖ **TIME DISPLAY key**
This switches the time display.
- ➙ **CLEAR key**
This erases the last tracks in a program.
- ➚ **DISPLAY**
- ➛ **CHECK key**
Press to check program contents.
- ➜ **Key**
When programming, this lets you input a number of consecutive tunes starting at a particular track number.
- ➝ **A ▶ B repeat key**
This key lets you define the beginning (A) and end (B) points of a section of music that you want played repeatedly.

Display window

- ➊ **Disc indicator (DISC)**
Confirms that a disc is in the tray.
- ➋ **Disc out indicator (OUT)**
This illuminates (red) when there is no disc in the tray.
- ➌ **A-B repeat indicator (A < B)**
- ➍ **REPEAT indicator (REPEAT)**
- ➎ **Time counter (TOTAL TIME, SINGLE TIME)**
- ➏ **Maximum track number indicator (MAX TNO.)**
Shows the highest track number found on the current disc.
- ➐ **Music calendar (1 - 20)**
Indicates the track (selection) numbers on the disc, or shows which selections are programmed for play.

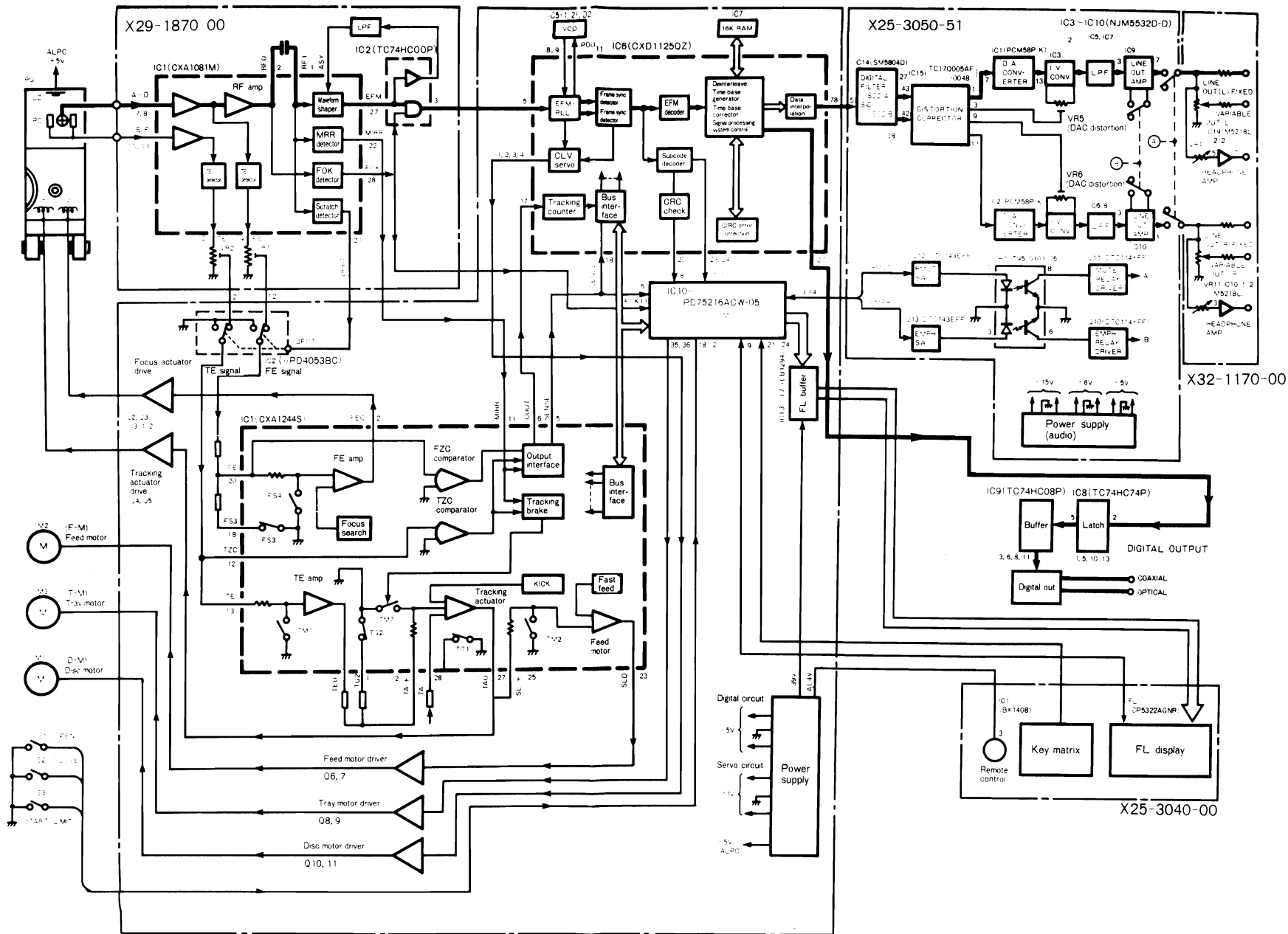


- ➐ **OUTPUT LEVEL indicator**
Six LEDs show the output level (of the signal from the VARIABLE jacks on the rear panel.) This can be adjusted by remote control or output level adjustment screw on the rear panel.

- ➑ **SPACE indicator (SPACE)**
- ➒ **Emphasis indicator (EMPHASIS)**
This confirms that the disc in play was recorded with high frequency emphasis.
- ➓ **Edit indicator (EDIT)**
- ➔ **Program check indicator (P.C.)**
Lights up when you check program contents.
- ➖ **Index number (INDEX)/program number (PNO.)**
Shows the current index number within the track. Shows the number of tracks during programming or when checking program contents.
- ➙ **Track number display (TRACK NO.)**
Shows the track number (according to the order of the selections on the disc).

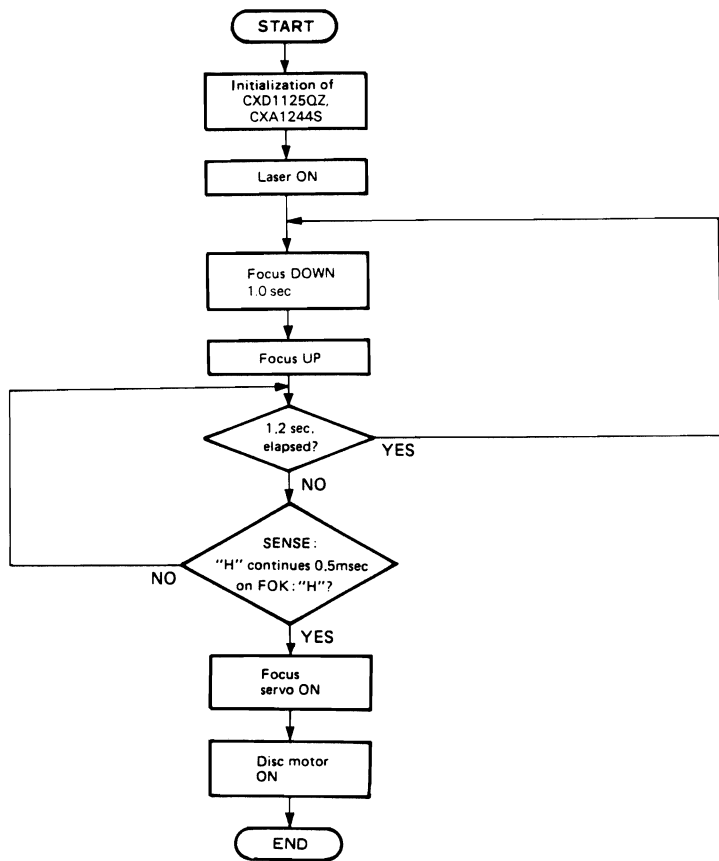
DP-1100SG : DP-1100SG

BLOCK DIAGRAM



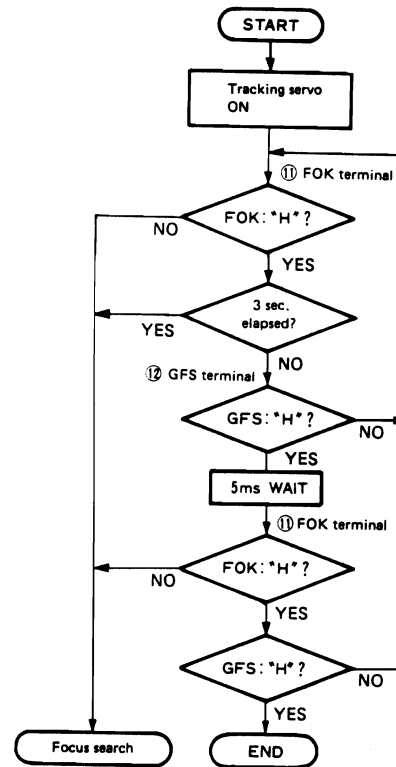
CIRCUIT DESCRIPTION

● Focus search & focus servo ON

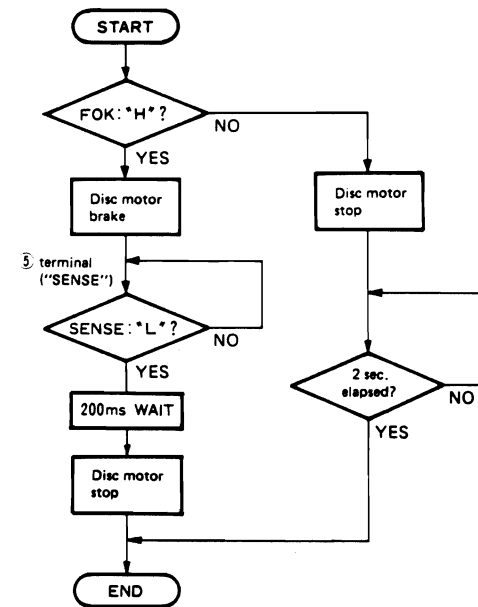


CIRCUIT DESCRIPTION

● Tracking servo ON

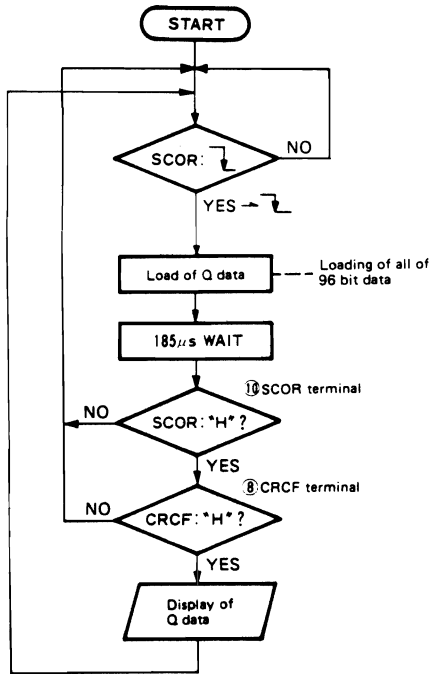


● Disc motor stop

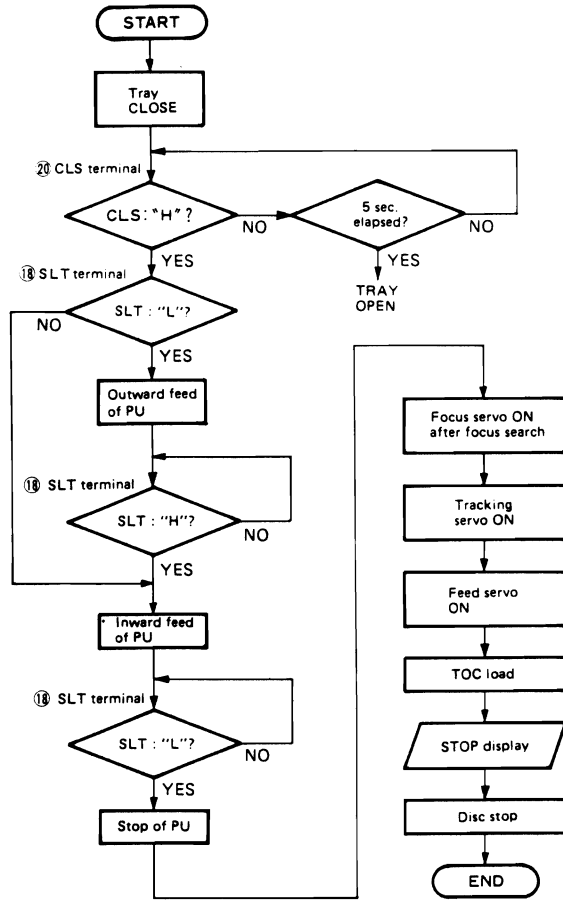


CIRCUIT DESCRIPTION

● From loading of Q data to display

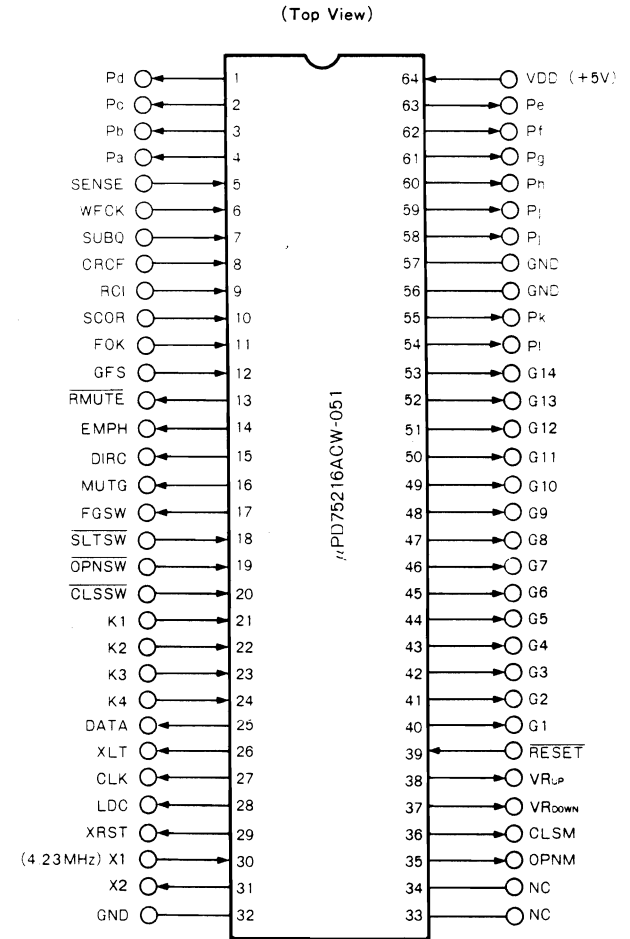


● Flow chart from the time the tray opens until the STOP indicator lights, after pressing the tray.



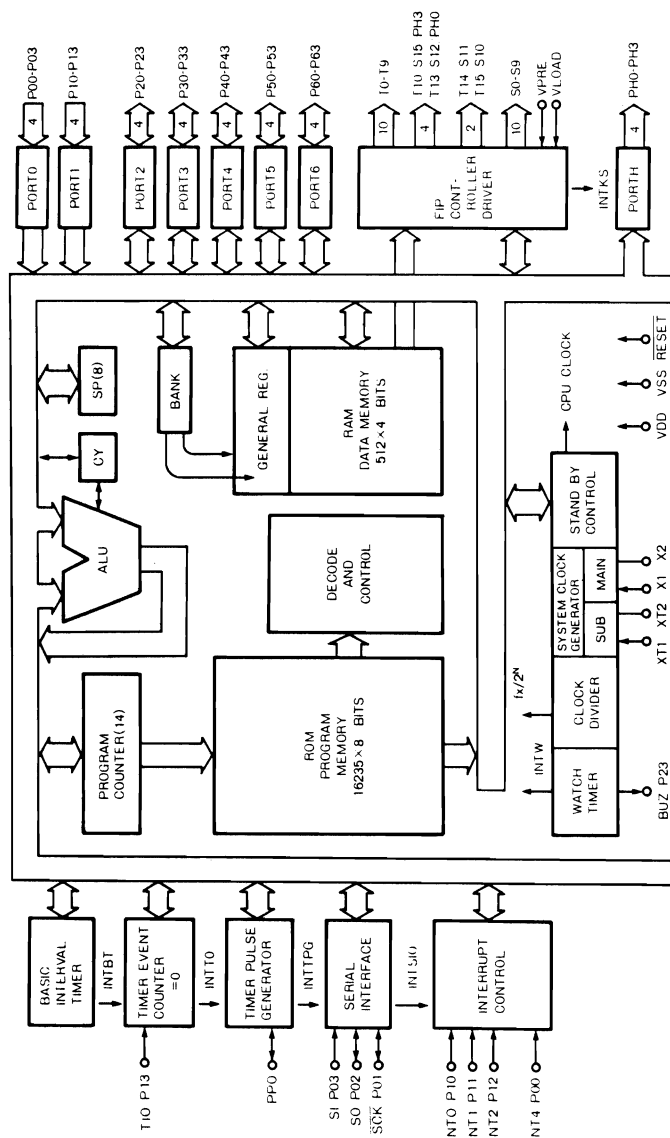
CIRCUIT DESCRIPTION

Microprocessor μ PD75216ACW-051 (X32-1170-00 : IC10)
Terminal connection diagram



CIRCUIT DESCRIPTION

μPD75216ACW-051 Block Diagram



CIRCUIT DESCRIPTION

Pin Function Table

Pin No.	Symbol	I/O	Pin Name	Functions
1 ~ 4	S3 ~ S0	O	Pd ~ Pa	FL display segment indication and key scan signal output
5	P00/INT4	I	SENSE	Sensing signal input (from CXD11250Z, CXA1244S)
6	P01/SCK	I	WFCK	Q data read-off clock input (from CXD11250Z)
7	P02/SO	I	SUBQ	Q data input (from CXD11250Z)
8	P03/SI	I	CRCF	Q data CRC OK ("H") input (from CXD11250Z)
9	P10/INT0	I	RCI	Remote control signal input
10	P11/INT0	I	SCOR	Q data sync signal input (from CXD11250Z)
11	P12/INT0	I	FOK	Focus OK ("H") input (from CXA1081M)
12	P13/T10	I	GFS	EFM sync OK ("H") input (from CXD11250Z)
13	P20	O	MUTE	Relay mute ON/OFF ("L"/"H")
14	P21	O	EMPH	Emphasis ON/OFF ("H"/"L")
15	P22	O	DIRC	DIRC signal/output (to CXA1244S)
16	P23	O	MUTG	MUTG signal output, Mute ON/OFF ("H"/"L") (to CXD11250Z)
17	P30	O	FGSW	Focus gain switch signal output
18	P31	I	SLT SW	Start limit switch signal input (SW ON = "L")
19	P32	I	OPN SW	Tray open switch signal input (SW ON = "L")
20	P33	I	CLS SW	Tray close switch signal input (SW ON = "L")
21	P60	I	K1	Key input for front panel
22	P61	I	K2	
23	P62	I	K3	
24	P63	I	K4	
25	P40	O	DATA	Control data signal output (to CXD11250Z, CXA1244S)
26	P41	O	XLT	Control data latch signal output (to CXD11250Z, CXA1244S)
27	P42	O	CLK	Control data clock signal output (to CXD11250Z, CXA1244S)
28	P43	O	LDC	Laser ON/OFF ("H"/"L") signal output
29	PPO	O	XRST	Control reset signal output (to CXD11250Z, CXA1244S)
30	X1	I	X1	Clock input pin (1/2 clock of CXD11250Z) (Oscillating frequency 4.2336 MHz)
31	X2	O	X2	
32	Vss	-	Vss	GND (ground)
35	P50	O	OPNM	Tray open/close signal output Normal (OPNM = "L", CLSM = "L") Open (OPNM = "H", CLSM = "L") Close (OPNM = "L", CLSM = "H")
36	P51	O	CLSM	
37	P52	O	V _R DOWN	
38	P53	O	V _R UP	Motor volume level up signal output
39	RESET	I	RESET	Reset signal input
40 ~ 53	T0 ~ T13/PH0	O	G ~ G14	FL display digit indication output
54	T14/S11	O	PI	FL display segment indication output
55	T15/S10	O	Pk	(Pt is also used for key scan)
56	VLOAD	I	VLOAD	GND (ground)
57	VPRE	I	VPRE	GND (ground)
58 ~ 63	S9 ~ S4	O	P ~ Pe	FL display segment indication and key scan signal output
64	VDD	I	VDD	+5 V power supply

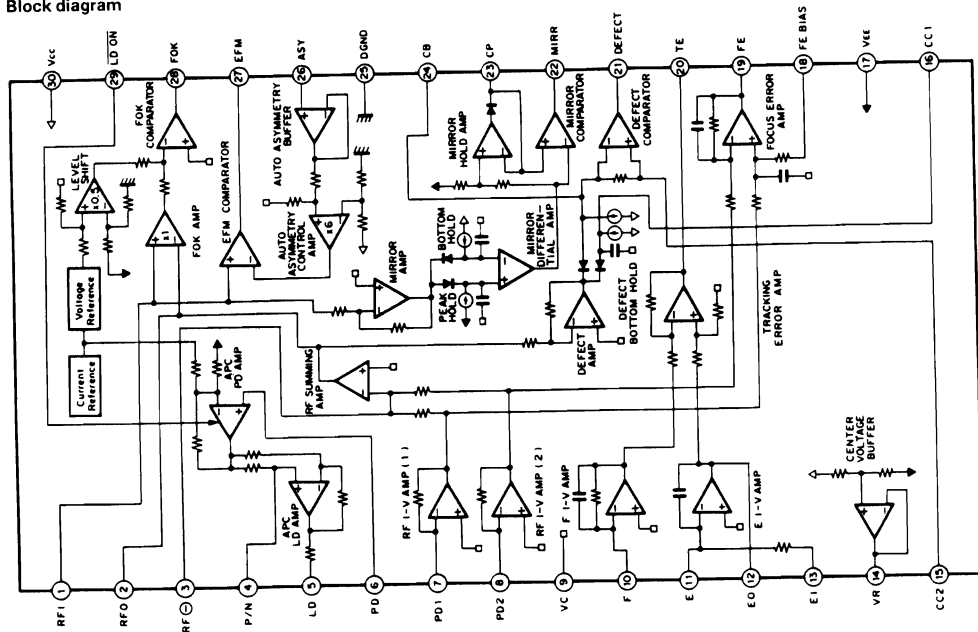
CIRCUIT DESCRIPTION

RF amplifier CXA1081M (X29-1870-00 : IC1)

The CXA1081M supplies the following functions as required for controlling the RF amp in the compact disc player.

- RF amp
- Focusing error amp
- Tracking error amp
- APC circuit
- Auto asymmetry control amp
- Focus OK detection circuit
- Mirror detection circuit
- Defect detection circuit
- EFM comparator

Block diagram



CIRCUIT DESCRIPTION

Explanation of terminals

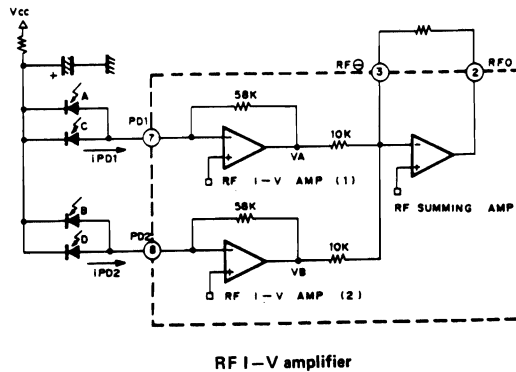
Terminal No.	Terminal name	I/O	Function
1	RF1	I	Input pin of the C-coupled signal output from the RF summing amp.
2	RFO	O	Check point of eye pattern for the RF summing amp output pin.
3	RF ⊖	I	RF summing amp feedback input pin.
4	P/N	I	P-sub/L-sub select pin of LD. (DC voltage: in N-sub mode)
5	LD	O	APC LD amp output pin. (DC voltage: PD open in N-sub mode)
6	PD	I	APC PD amp input pin. (DC voltage: open)
7	PD1	I	RF I-V amp (1) invert input pin. Current input by connecting to PIN diode A + C.
8	PD2	I	RF I-V amp (2) invert input pin. Current input by connecting to PIN diode B + D.
9	VC	-	Connected to GND when using a positive (+)/negative (-) dual-voltage power supply. Connected to VR (pin 14) when using a single-voltage power supply.
10	F	I	F I-V amp invert input pin. Current input by connecting to PIN diode F.
11	E	I	E I-V amp invert input pin. Current input by connecting to PIN diode E.
12	EO	O	E I-V amp output pin.
13	EI	I	E I-V amp feedback input pin. For E I-V amp gain adjustment.
14	VR	O	DC voltage output pin of (Vcc + VEE)/2.
15	CC2	I	Input pin of the C-coupled signal output from the defect bottom hold.
16	CC1	O	Defect bottom hold output pin.
17	VEE	-	Connected to the negative power supply when using a positive (+)/negative (-) dual-voltage power supply. Connected to GND when using a single-voltage power supply.
18	FE BIAS	I	Bias pin at the focus error amp non-invert side. For CMR adjustment of the focus error amp.
19	FE	O	Focus error amp output pin.
20	TE	O	Tracking error amp output pin.
21	DEFECT	O	Defect comparator output pin. (DC voltage: connected to a 10kΩ load).
22	MIRR	O	Mirror comparator output pin. (DC voltage: connected to a 10kΩ load).
23	CP	I	Mirror hold capacitor output pin. Mirror comparator non-invert input.
24	CB	I	Defect bottom hold capacitor connect pin.
25	DGND	-	Connected to GND when using a positive (+)/negative (-) dual-voltage power supply. Connected to GND (VEE) when using a single-voltage power supply.
26	ASY	I	Auto asymmetry control input pin.
27	EFM	O	EFM comparator output pin. (DC voltage: connected to a 10kΩ load).
28	FOK	O	FOK comparator output pin. (DC voltage: connected to a 10kΩ load).
29	LD ON	I	LD ON/OFF select pin. (DC voltage: when LD ON).
30	Vcc	-	Positive power supply.

CIRCUIT DESCRIPTION

Explanation of function

● RF amp

The photodiode current input to the input pins (PD1, PD2) is converted to a voltage by an equivalent resistance of 58kΩ in RF I-V amp (1) and (2) respectively. The voltage which is converted from the current of the photodiode (A + B + C + D) is added in the RF summing amp and is output from the RFO pin. The eye pattern can be checked at this pin.



RF I-V amplifier

The low frequency component of the RFO output voltage, V_{RFO} is represented by the following equation:

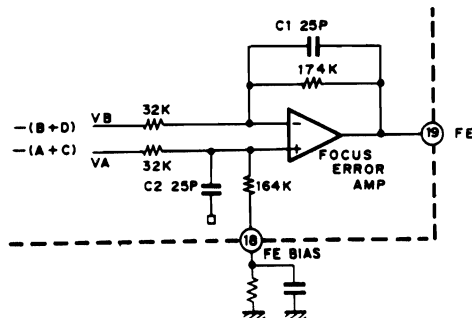
$$V_{RFO} = 2.2 \times (V_A + V_B) \\ = 127.6k\Omega \times (i_{PD1} + i_{PD2})$$

● Focus error amp

The difference between the RF I-V amp (1) output (V_A) and the RF I-V amp (2) output (V_B) is calculated, and the current of the photodiode (A + C - B - D) is converted to a voltage and output.

The FE output voltage (low frequency) is represented by the following equation:

$$V_{FE} = 5.4 \times (V_A - V_B) \\ = (i_{PD2} - i_{PD1}) \times 315.4k\Omega$$



CIRCUIT DESCRIPTION

● Tracking error amp

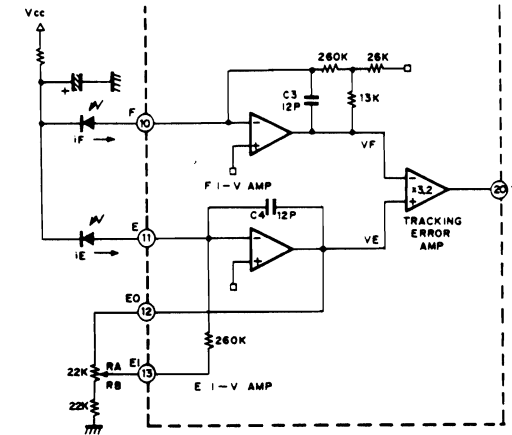
The current from the side spot photodiodes is input to pins E and F and is converted to a voltage by the E I-V amp and F I-V amp respectively. That is:

$$V_F = i_F \times 403k\Omega$$

$$V_E = i_E \times 260k\Omega \times R_A / (R_B + 22k) + (R_A + 260k)$$

The difference between the E I-V amp and the F I-V amp is calculated by the tracking error amp, and the photodiode (E-F) current is converted to a voltage and output.

$$V_{TE} = (V_E - V_F) \times 3.2 \\ = (i_E - i_F) \times 1290k\Omega$$



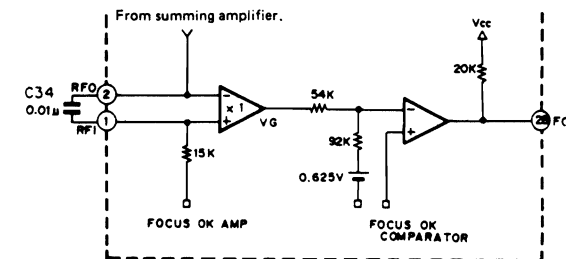
● Focus OK circuit

The focus OK circuit creates a timing window, turning the focusing servo ON with the focus search status.

While the RF signal is present at pin 2, its HPF output is present at pin 1. At the same time, the LPF output (opposite phase) of the focus OK amp is obtained.

The focus OK output is inverted when $V_{RF1} - V_{RFO} = -0.37V$.

C34 is used to determine the time constants of the EFM comparator, the HPF in the mirror circuit, and the LPF in the focus OK amp. Normally, C34 = 0.01μF is selected, with $f_c = 1kHz$. This will prevent degradation of the block error rate due to an RF envelope lack caused by cracks, etc. on the disc.



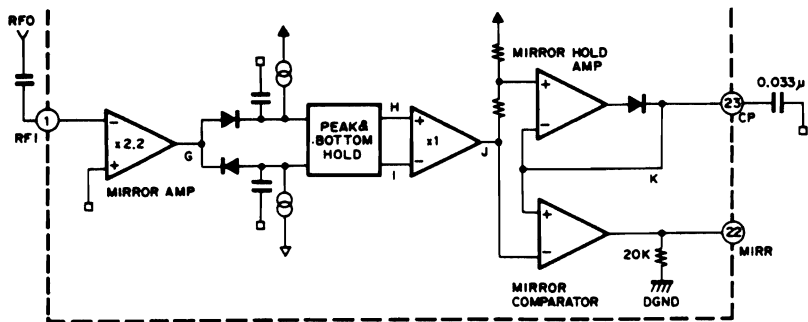
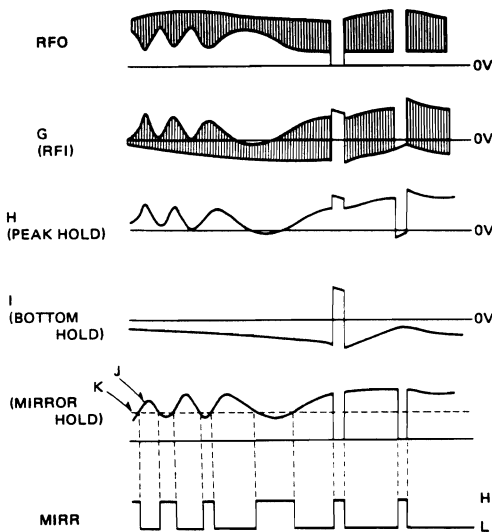
CIRCUIT DESCRIPTION

● Mirror circuit

In the mirror circuit, after the RFI signal is amplified, both peak and bottom holds are held by a time constant which can follow a traverse of 30kHz, while only the bottom hold is held by a time constant which can follow a cyclic period envelope variation respectively.

These peak/bottom hold signals, H and I are differentially amplified to obtain the DC-reproduced envelope signal J.

This signal is compared with signal K, that the 2/3 level of the peak value is peak held by a large time constant so that the mirror output is obtained. That is, the mirror output goes "L" on the disc tracks and goes "H" between tracks (mirror section). In addition, the output goes "H" when a defect is detected. The time constant of the mirror hold should be quite larger when compared with the traverse signal.



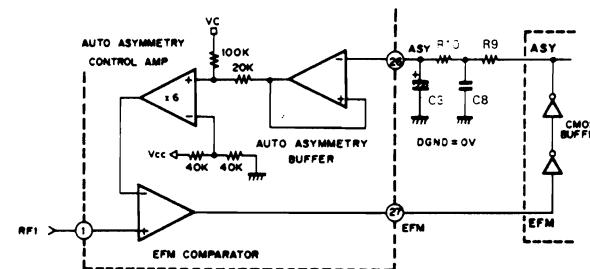
CIRCUIT DESCRIPTION

● EFM comparator

The EFM comparator converts the RF signal into a binary coded signal. Since asymmetry caused by dispersion when manufacturing the discs cannot be reduced by AC coupling only, the reference voltage of the EFM comparator is controlled using the characteristics that the present probability of a 1 or 0 is 50% each for the binary coded EFM signal.

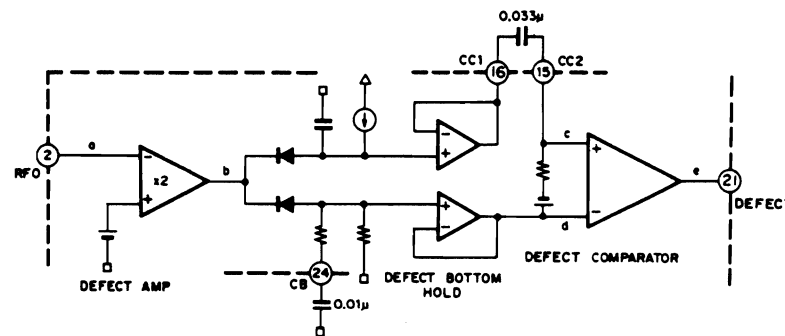
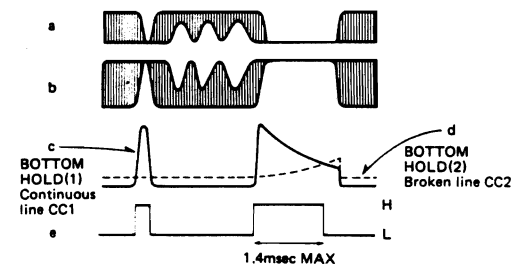
The EFM comparator is designed as a current switching type, and the "H" and "L" levels are not equal to the power voltages. Therefore, feedback is required via a CMOS buffer.

R9, R10, C3 and C8 constitute a LPF to obtain the DC component of $(V_{CC}-DGND)/2$ (V). If the cut-off frequency (fc) is set to more than 500Hz, leakage of the EFM low frequency signals will be greatly increased and will result in a degradation of the block error rate.



● Defect circuit

After inverting the RFI signal, the defect circuit bottom holds with the two long/short time constants. The bottom hold with a shorter time constant responds to a mirror defect of more than 0.1msec on the disc, and the bottom hold with a longer time constant holds the mirror level obtained immediately before the defective section. These signals are C-coupled, then differentiated with level shifting. The signals are compared with each other to generate the mirror defect detecting signals.



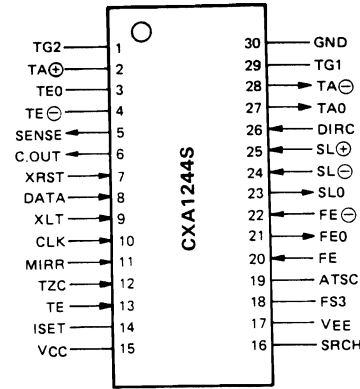
CIRCUIT DESCRIPTION

Servo signal processor CXA1244S (X32-1170-00 : IC1)

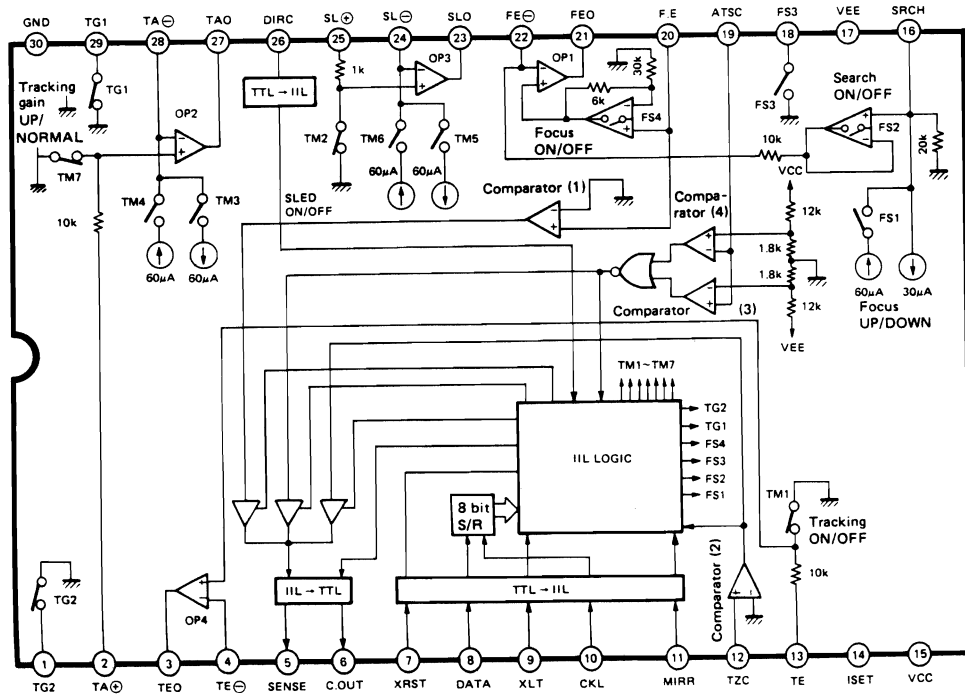
CXA1244S is a bipolar IC developed for servo of compact disc (CD) players, and it provides the following functions.

- Tracking control (servo ON/OFF, single track jump, multiple track jump, gain control, phase compensation control, brake circuit)
- Sled control (servo ON/OFF, fast forward, fast reverse)

Terminal connection diagram



Block diagram



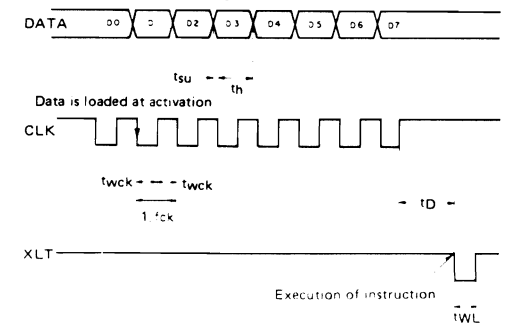
Explanation of terminals

Terminal No.	Terminal name	I/O	Functions
1	TG2		Tracking amplifier gain switching terminal. GND level.
2	TA ⊕		Non-inverted input of operational amplifier 2.
3	TE0		Output of operational amplifier 4.
4	TE ⊖		Inverted input of operational amplifier 4.
5	SENSE	O	Output of SSP internal status that corresponds to ADDRESS of CPU → SSP. (Changes in accordance with ADDRESS content of internal serial register.) See Note 1.
6	C. OUT	O	Signal output for counting number of tracks at the time of high speed access.
7	XRST	I	All internal registers are cleared when CPU → SSP "L". Connected with CPU RESET. See Note 2.
8	DATA	I	Serial data transmission of CPU → SSP. Input is made from LSB, D0~D7.
9	XLT	I	Latch of serial data of CPU → SSP. (The contents of internal serial register are transmitted to each address decoded latch.) Transmission at "L". Change to "H" occurs immediately after execution because no edge trigger is produced.
10	CLK	I	CPU → SSP serial data transmission block. Data is read at falling. "H" level before and after transmission.
11	MIRR	I	Mirror signal input from RF amplifier.
12	TZC	I	Tracking error signal is input with C couple. The time constant is determined by one single track jump, but it is usually around 2kHz.
13	TE	I	Tracking error signal input.
14	ISET		Setting of current level for determining focus search voltage, tracking jump voltage and thread feed voltage.
15	Vcc		Power supply terminal. Normally +5V.
16	SRCH		The condenser for determining the time constant of charge/discharge waveform for focus search is connected.
17	VEE		Power supply terminal. Normally -5V.
18	FS3		Focus amplifier gain switching terminal. GND level.
19	ATSC		Such information that a mechanical shock was applied to the player is input. Simply, a tracking error is input through BPF. In this equipment it is connected to GND level and is not used.
20	FE	I	Input of focus error signal.
21	FE0	O	Output of operational amplifier 1.
22	FE ⊖	I	Inverted input of operational amplifier 1.
23	SL0	O	Output of operational output 3.
24	SL ⊖	I	Inverted input of operational amplifier 3.
25	SL ⊕	I	Non-inverted input of operational amplifier 3.
26	DIRC	I	Used at the time of one track jump. Normally "H". The direction of the track jump pulse is reversed with "L". Setting is made in the normal tracking mode by changing to "H". "L" for a fixed length of time with detection of activation, deactivation of TZC.
27	TA0	O	Output of operational amplifier 2.
28	TA ⊖	O	Inverted input of operational amplifier 2.
29	TG1		Tracking amplifier gain switching terminal. GND level.
30	GND		GND terminal of IC.

Note 1 : SENSE terminal output

Serial data upper 4 bits	ADDRESS content	SENSE terminal output	Explanation
0 0 0 0	FOCUS CONTROL	FZC	"H" when focus zero cross. Focus error voltage is DV (2mV) higher. Used as the signal of FOCUS PLUS operation.
0 0 0 1	TRACKING CONTROL	AS	"H" when the ATSC input level exceeds the wind comparator level (V _{th} = V _{CC} × 13%). Bursts are used in this equipment.
1 1 1 0	TRACKING MODE	TZC	Judgement output of positive or negative of tracking error cross tracking error. When set at the time of single track jump, DIRC is used. The direction of the track jump pulse is reversed with "L". Setting is made in the normal tracking mode by changing to "H". "L" for a fixed length of time with detection of activation, deactivation of TZC.

Note 2 : Digital unit timing chart



CIRCUIT DESCRIPTION

System control

COMMAND	ADDRESS				DATA				SENSE
	D7	D6	D5	D4	D3	D2	D1	D0	
FOCUS CONTROL	0	0	0	0	FS4 FOCUS ON	FS3 GAIN DOWN	FS2 SEARCH ON	FS1 SEARCH UP	FZC
TRACKING CONTROL	0	0	0	1	ANTI SHOCK	BREAK ON	TG2 GAIN	TG1* SET	AS
TRACKING MODE	0	0	1	0	TRACKING* MODE		SLED* MODE		TZC

GAIN SET* TG1, TG2 may be set independently.
In the case of ANTI SHOCK = 1 (00011XXX), both TG1, TG2 are inverted when ANTI SHOCK = "H".

TRACKING MODE*

	D3	D2
OFF	0	0
SERVO ON	0	1
FWD JUMP	1	0
REV JUMP	1	1

SLED MODE*

	D1	D0
OFF	0	0
SERVO ON	0	1
FWD MOVE	1	0
REV MOVE	1	1

Note : The antishock circuit is not used in this equipment.

CIRCUIT DESCRIPTION

Serial data truth value table

Serial data	Hexa-decimal	Function
FOCUS CONTROL		FS = 4321
00000000	S00	0000
00000001	S01	0001
00000010	S02	0010
00000011	S03	0011
00000100	S04	0100
00000101	S05	0101
00000110	S06	0110
00000111	S07	0111
00001000	S08	1000
00001001	S09	1001
00001010	S0A	1010
00001011	S0B	1011
00001100	S0C	1100
00001101	S0D	1101
00001110	S0E	1110
00001111	S0F	1111

TRACKING CONTROL		D2 (Brake)	AS = 0 TG = 2 1	AS = 1 TG = 2 1
00010000	S10	0	0 0	0 0
00010001	S11	0	0 1	0 1
00010010	S12	0	1 0	1 0
00010011	S13	0	1 1	1 1
00010100	S14	1	0 0	0 0
00010101	S15	1	0 1	0 1
00010110	S16	1	1 0	1 0
00010111	S17	1	1 1	1 1
00011000	S18	0	0 0	1 1
00011001	S19	0	0 1	1 0
00011010	S1A	0	1 0	0 1
00011011	S1B	0	1 1	0 0
00011100	S1C	1	0 0	1 1
00011101	S1D	1	0 1	1 0
00011110	S1E	1	1 0	0 1
00011111	S1F	1	1 1	0 0

AS : ANTI SHOCK

TRACKING MODE		DC = 1 TM = 654321	DC = 1 654321	DC = 1 654321
00100000	S20	000000	001000	000011
00100001	S21	000010	001010	000011
00100010	S22	010000	011000	100001
00100011	S23	100000	101000	100001
00100100	S24	000001	000100	000011
00100101	S25	000011	000110	000011
00100110	S26	010001	010100	100001
00100111	S27	100001	100100	100001
00101000	S28	000100	001000	000001
00101001	S29	000110	001010	000011
00101010	S2A	010100	011000	100001
00101011	S2B	100100	101000	100001
00101100	S2C	001000	000100	000011
00101101	S2D	001010	000110	000011
00101110	S2E	011000	010100	100001
00101111	S2F	101000	100100	100001

DC : DIRC input terminal

CIRCUIT DESCRIPTION

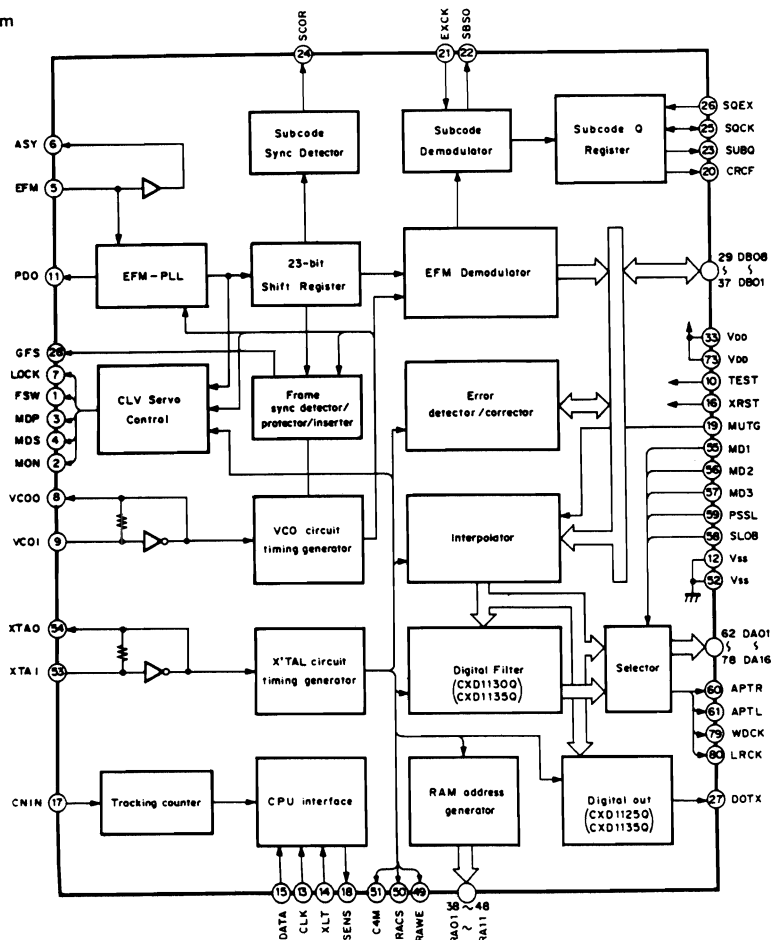
Digital signal processing LSI CXD1125QZ (X32-1170-00 : IC6)

The CXD1125QZ is the digital signal processing LSI for the compact disc player, and has the following functions. All the digital signals for reproduction can be processed internally with this one-chip design.

- Bit clock reproduction by an EFM-PLL circuit.
- EFM data demodulation.
- Frame sync signal detection, protection and insertion.
- Powerful error detection and correction.

- Interpolation with average value or by holding the previous value.
- Demodulation of sub code signal or error detection of sub code Q.
- Spindle motor CLV servo.
- 8-bit tracking counter.
- CPU interface with a serial bus.
- Sub code Q register.
- D/A interface output.

Block diagram



CIRCUIT DESCRIPTION

Explanation of terminals

Terminal No.	Terminal name	I/O	Function
1	FSW	O	Time constant switching output of output filter of spindle motor.
2	MON	O	ON/OFF control output of spindle motor.
3	MDP	O	Drive output of spindle motor. Rough speed control in CLV-S mode and phase control in CLV-P mode.
4	MDS	O	Drive output of spindle motor. Speed control in CLV-P mode.
5	EFM	I	EFM signal input from RF amplifier.
6	ASY	O	Output for controlling the slice level of EFM signal.
7	LOCK	O	Samples the GFS signal with WFCK/16, and outputs "H" when the level is high. When it is "L" for eight times, in a row, outputs "L".
8	VCOO	O	VCO output. f = 8.6436MHz when locked to EFM signal.
9	VCOI	I	VCO input.
10	TEST	I (0V)	
11	PDO	O	Phase comparison output of EFM signal and VCO/2.
12	Vss	-	GND (0V)
13	CLK	I	Serial data transmission clock input from CPU. Data is latched at rising edge of a clock.
14	XLT	I	Latch input from CPU. Data (serial data from CPU) from the 8 bit shift register is latched in each register.
15	DATA	I	Serial data input from CPU.
16	XRST	I	System reset input. Reset at "L".
17	CNIN	O	Input of tracking pulse.
18	SENSE	O	Output of internal status in correspondence to the address.
19	MUTG	I	Muting input. In the case where ATTM of internal register A is "L", normal status when MUTG is "L" or soundless state when it is "H".
20	CRCF	O	Output of result of CRC check of sub code Q.
21	EXCK	I	Clock input for sub code serial output.
22	SBSO	O	Sub code Q read-off clock.
23	SUBQ	O	Sub code Q output.
24	SCOR	O	Sub code sync SO + SI output.
25	WFCK	O	Write Frame Clock output. f = 7.35kHz when the frame sync is locked.
28	CFS	O	Output of display of lock status of frame sync.
29	DB08	I/O	Data terminal of external RAM. DATA 8 (MSB)
30	DB07	I/O	Data terminal of external RAM. DATA 7
31	DB06	I/O	Data terminal of external RAM. DATA 6
32	DB05	I/O	Data terminal of external RAM. DATA 5
33	VDD	-	Power supply (+5V)
34	DB04	I/O	Data terminal of external RAM. DATA 4
35	DB03	I/O	Data terminal of external RAM. DATA 3
36	DB02	I/O	Data terminal of external RAM. DATA 2
37	DB01	I/O	Data terminal of external RAM. DATA 1 (LSB)
38	RA01	O	Address output of external RAM. ADDR01 (LSB)
39	RA02	O	Address output of external RAM. ADDR02
40	RA03	O	Address output of external RAM. ADDR03
41	RA04	O	Address output of external RAM. ADDR04
42	RA05	O	Address output of external RAM. ADDR05
43	RA06	O	Address output of external RAM. ADDR06
44	RA07	O	Address output of external RAM. ADDR07
45	RA08	O	Address output of external RAM. ADDR08
46	RA09	O	Address output of external RAM. ADDR09
47	RA10	O	Address output of external RAM. ADDR10
48	RA11	O	Address output of external RAM. ADDR11 (MSB)
49	RAW	O	Write Enable signal output to external RAM, (active at "L").
50	RACS	O	Chip select signal output to external RAM. (active at "L").

CIRCUIT DESCRIPTION

CIRCUIT DESCRIPTION

Terminal No.	Terminal name	I/O	Function
51	C4M	O	Crystal dividing output. $f = 4.2336\text{MHz}$.
52	Vss	-	GND (0V).
53	XTAI	I	Crystal oscillator input. $f = 8.4672\text{MHz}$ or 16.9344MHz depending on the mode selected.
54	XTAO	O	Crystal oscillator output. $f = 8.4672\text{MHz}$ or 16.9344MHz depending on the mode selected.
55	MD1	I	Mode select input 1.
56	MD2	I	Mode select input 2.
57	MD3	I	Mode select input 3.
58	SLOB	I	Audio data output code select input. 2's complement output when "L", offset binary output when "H".
59	PSSL	I	Audio data output mode select output. Serial output when "L", parallel output when "H".
60	APTR	O	Aperture compensation control output. "H" when R-ch.
61	APTL	O	Aperture compensation control output. "H" when L-ch.
62	DA01	O	DA01 (parallel audio data LSB) output when PSSL = "H", C1F2 output when PSSL = "L".
63	DA02	O	DA02 output when PSSL = "H", C1F1 output when PSSL = "L".
64	DA03	O	DA03 output when PSSL = "H", C2F1 output when PSSL = "L".
65	DA04	O	DA04 output when PSSL = "H", C2F2 output when PSSL = "L".
66	DA05	O	DA05 output when PSSL = "H", C2FL output when PSSL = "L".
67	DA06	O	DA06 output when PSSL = "H", C2PO output when PSSL = "L".
68	DA07	O	DA07 output when PSSL = "H", RFCK output when PSSL = "L".
69	DA08	O	DA08 output when PSSL = "H", WFCK output when PSSL = "L".
70	DA09	O	DA09 output when PSSL = "H", PLCK output when PSSL = "L".
71	DA10	O	DA10 output when PSSL = "H", UGFS output when PSSL = "L".
72	DA11	O	DA11 output when PSSL = "H", GTOP output when PSSL = "L".
73	VDD	-	Power supply (+5V).
74	DA12	O	DA12 output when PSSL = "H", RAOV output when PSSL = "L".
75	DA13	O	DA13 output when PSSL = "H", C4LR output when PSSL = "L".
76	DA14	O	DA14 output when PSSL = "H", C210 output when PSSL = "L".
77	DA15	O	DA15 output when PSSL = "H", C21O output when PSSL = "L".
78	DA16	O	DA16 (parallel audio data MSB) output when PSSL = "H", DATA output when PSSL = "L".
79	WDCK	O	Strobe signal output. 88.2kHz.
80	LRCK	O	Strobe signal output. 44.1kHz.

Notes:
 C1F1 : Error correction status monitor output for C1 decode.
 C1F2 : }
 C2F1 : } Error correction status monitor output for C2 decode.
 C2F2 : }
 C2PO : C2 pointer signal.
 C2FL : Correction status output. Goes "H" when the currently corrected C2 series data cannot be corrected.
 RFCK : Read frame clock output. 7.35MHz when locked to the crystal line.
 WFCK : Write frame clock output. 7.35MHz when locked to the crystal line.

PLCK : VCO/2 output. $f = 4.3218\text{MHz}$ when locked to the EFM signal.
 UGFS : Non-protected frame sync pattern output.
 GTOP : Frame sync protect status display output.
 RAOV : ± 4 frame jitter absorption RAM overflow and underflow display output.
 C4LR : Strobe signal. 176.4kHz.
 C210 : C21O invert output.
 C21O : Bit clock output. 2.1168MHz.
 DATA : Audio signal serial data output.

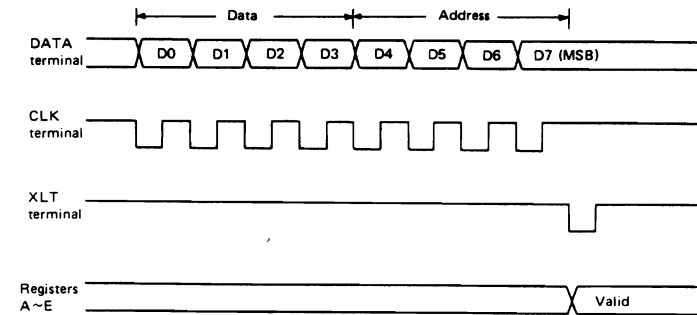
Explanation of functions

● CPU interface

1) Data input

Each register may be set by input of 4 bit address, and 4 bit data from LSB in the timing that is shown in Fig. 6-2

to three terminals, XLT, CLK and DATA. The address and data of each terminal are as shown in Table 6-2, and their functions are as follows. The contents of each register become entirely 0 when XRST = "L".



Timing chart for data input

2) Registers

○ Register 9 – New function control

Controls the new functions added to the CX23035.

D3 : ZCMT Switches the zero cross mute function ON/OFF. Details are described in "Interpolation and Mute, Attenuate".

D2 : HZPD One of the defect countermeasures. Switches ON/OFF the function which makes the PD0 pin a high impedance (Z) for a maximum of 0.55ms from the rising edge of GFS. Details are described in "Countermeasures to defects".

D1 : NCLV Switches between the old CLV-P servo and the new CLV-P servo by comparison with newly added base counter. Details are described in "CLV servo control".

D0 : CRCQ Switches ON/OFF the function which outputs the CRCF data to the SUBQ pin from the rising edge of SCOR to the trailing edge of SQCK. Details are described in "5) Subcode output".

○ Register A – Sync. protection, attenuator control

D3 : GSEM } Provided for switching frame sync. protection characteristics in correspondence to the time of playback and time of access. Details will be described in the paragraph of "EFM demodulation".
 D2 : GSEL }
 D1 : WSEL }
 D0 : ATTM

D0 : ATTM Used for attenuating audio signals by 12dB, and the details will be described in the paragraph of "D/A interface".

○ Registers B and C – Counter set, more significant 4 bits (register C) and less significant 4 bits (register B) these registers are used for setting the tracking count value. the data of registers B and C are preset in the counter through the 4 bit buffer register assigned by address.

Accordingly, when data of either register B or C is input, the contents of both registers are preset in the counter simultaneously as 8 bit data (either buffer register is of "OLD" data.)

D3 : DIV The dividing ratio of RFCK and WFCK in CLV-P mode is fixed, and the phase is compared with RFCK/4 or WFCK/4 respectively, regardless of the status of D3, then output from the MDP pin.

○ Register D-CLV control

D3 : DIV Used for setting the frequency dividing ratio of RFCK, WFCK in the CLV-P mode. When D3 = 0., phase comparison of RFCK/4 and WFCK/4 is made, and when D3 = 1, phase comparison of RFCK/8 and WFCK/8 is made, and output is made out of MDP terminal in each case.

D2 : TB Used for determining the period of bottom hold in the CLV-S and CLV-H modes. Bottom hold is made in the period of RFCK/32 when D2 = 0 or in the period of RFCK/16 when D2 = 1.

D1 : Tp Used for setting the period of peak hold in the CLV-S mode. Peak hold is made in the period of RFCK/4 when D1 = 0 or in the period of RFCK/2 when D1 = 1.

D0 : GAIN Used for setting the gain of MDP terminal output in the CLV-S and CLV-H modes. It is -12dB (time of 3/4 out of the period of RFCK/2 is of high impedance) when D0 = 0 or is 0dB when D0 = 1.

CIRCUIT DESCRIPTION

o Register E-CLV mode

It is as shown in Table 6-2.

The details of each mode will be described in the paragraph of CLV servo control.

Register name	Command	Address D7~D4	Data				SENSE terminal
			D3	D2	D1	D0	
9*1	New function control	1 0 0 1	ZCMT	HZPD	NCLV	CRCQ	Z
A*2	Sync protection, attenuator control	1 0 1 0	GSEM	GSEL	WSEL	ATTM	Z
B	Counter set, Less significant 4 bits	1 0 1 1	Tc3	Tc2	Tc1	Tc0	COMPLETE
C	Counter set, More significant 4 bits	1 1 0 0	Tc7	Tc6	Tc5	Tc4	COUNT
D*3	CLV control	1 1 0 1	DIV	TB	TP	GAIN	Z
E*4	CLV mode	1 1 1 0	CLV mode				Pw ≥ 64

*1 Register 9

		Dn = 0	Dn = 1
ZCMT	D3	Zero-cross MUTE off	Zero-cross MUTE on
HZPD	D2	PDC pin is always active	PDC pin is "Z" at the trailing edge of GFS
NCLV	D1	CLV-P servo for the frame sync signal	CLV-P servo for the base counter
CRCQ	D0	CRCF is not superimposed on SUBQ	SUBQ = CRCF at the raising edge of SCOR

*2 Register A

GSEM	GSEL	Frame
0	0	2
0	1	4
1	0	8
1	1	13

WSEL	Clock
0	±3
1	±7

ATTM	MUTG terminal	dB
0	0	0
0	1	-∞
1	0	-12
1	1	-12

*3 Register D

DIV	D3	D2	Description
0	0	RFCK/4 & WFCK/4	Phase comparison frequency in CLV-P mode
	1	RFCK/8 & WFCK/8	
TB	0	RFCK/32	Bottom hold period in CLV-S, CLV-H mode
	1	RFCK/16	
TP	0	RFCK/4	Peak hold frequency in CLV-S mode
	1	RFCK/2	
GAIN	0	-12dB	Gain at MDP terminal in CLV-S, CLV-H mode
	1	0dB	

*4 Register E

Mode	D3~D0	MDP terminal	MDS terminal	FSW terminal	MON terminal
STOP	0 0 0 0	L	Z	L	L
KICK	1 0 0 0	H	Z	L	H
BRAKE	1 0 1 0	L	Z	L	H
CLV-S	1 1 1 0	CLV-S	Z	L	H
CLV-H	1 1 0 0	CLV-H	Z	L	H
CLV-P	1 1 1 1	CLV-P	CLV-P	Z	H
CLV-A	0 1 1 0	CLV-S or CLV-P	Z or CLV-P	L or Z	H

Z: High impedance

List of registers

CIRCUIT DESCRIPTION

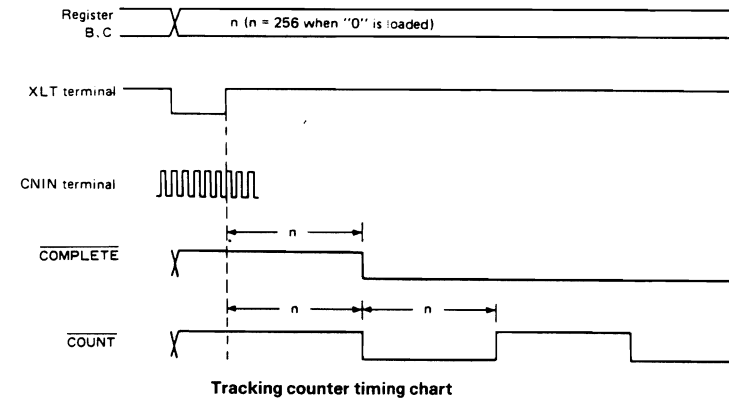
3) Tracking counter

This counter is provided for facilitating track jump. Load the number of tracks to be jumped in register B and C. Count of CNIN pulses is started at raising edge of XLT after it was loaded in either register B or C.

When n (n = 256 is meant when register B = register C =

0) is loaded in registers and the address is set at "B", a signal (COMPLETE) that is of HIGH level up to "n" pulses and is of LOW level after "n" pulses is output of SENSE terminal. When the address is set at "C", signal (COUNT) of CNIN/2n (Hz) is output.

The tracking counter timing chart is shown in Fig. 6-3.



Tracking counter timing chart

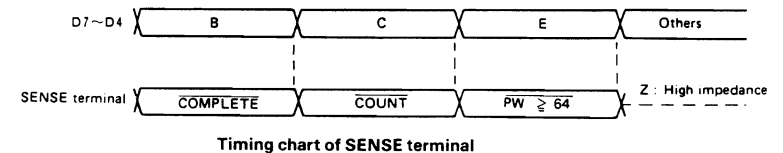
4) SENSE

The following signals are output from SENSE terminal depending on the address of D7~D4.

1. COMPLETE: Address is "B"; Shown in Fig. 6-3.
2. COUNT: Address is "C"; Shown in Fig. 6-3.
3. PW≥64: Address is "E"; this signal is of LOW level

when the pulse width after bottom hold is over 63, and is of HIGH level otherwise. It is used for detection of a drop in the speed of the spindle motor after braking and so on.

Note: Address setting is determined only by the data that corresponds to D4~D7 which can be input from DATA terminal shown in Fig. 6-2.



Timing chart of SENSE terminal

CIRCUIT DESCRIPTION

5) Sub code output

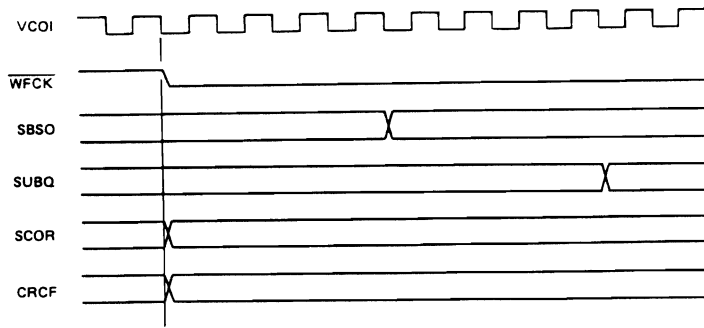
Sub codes P~W loaded in the 8 bit shift register are output out of SBSO terminal in accordance with the clock input through EXCK terminal. when SCOR terminal is "H", S0 - S1 signal is output.

Sub code Q is as follows, depending on the SQEX pin status.

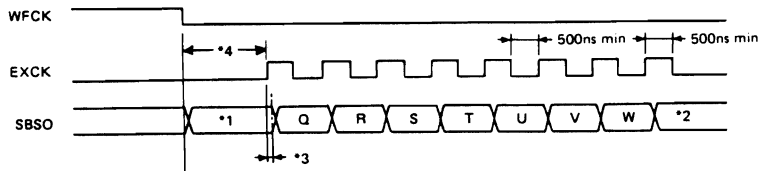
- (i) When the SQEX pin is "L", sub code Q is output from the SUBQ pin in synchronism with the WFCK signal in the same way as for the CX23035. The WFCK is also output from the SQCK pin.
- (ii) When the SQEX pin is "H", sub code Q is output from the SUBQ pin in synchronism with the external clock

(as from the microprocessor). Two 80-bit shift registers, for reading and writing, are incorporated, and while the microprocessor reads, the new sub code Q is written to another register. The microprocessor is interrupted from the outside at the rising edge of the SCOR pin, and after checking the CRCF flag (output to the CRCF pin, or the SUBQ pin when the CRCQ flag is "1"), the CRCF is checked. If CRCF = "H", a shift lock is output and the new sub code Q is read. After the LSB side is replaced with the MSB side by a unit of 4 bits, the data is stored in register. As the microprocessor serially inputs from the LSB first, replacing the 4 bits of data is unnecessary.

(a) Timing of SBSO, SUBQ, SCOR, CRCF



(b) Timing of SBSO, EXCK



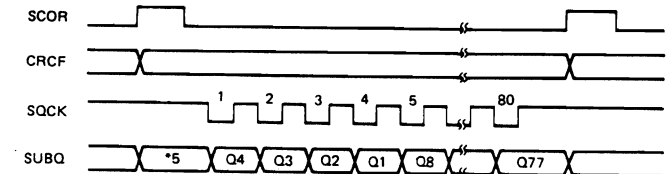
- *1 : Sub code P is output when SCOR is 0. S0 - S1 is output when SCOR is 1.
- *2 : SBSO is 0 when 8 or more pulses are input to EXCK.
- *3 : $4T \sim 6T$ if the period of VCO is expressed as T.
- *4 : Make EXCK low for $10\mu s$ from the rising edge of WFCK. One time period of T = 8.6436MHz.

(1) Timing chart of sub code outputs

CIRCUIT DESCRIPTION

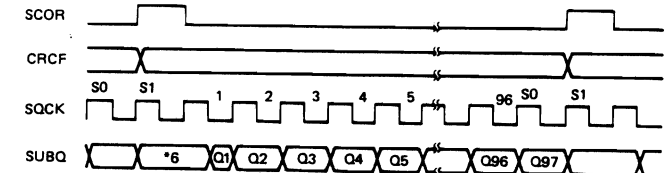
(c) Timing of SCOR, CRCF, SQCK, SUBQ

SQEX= "H" level



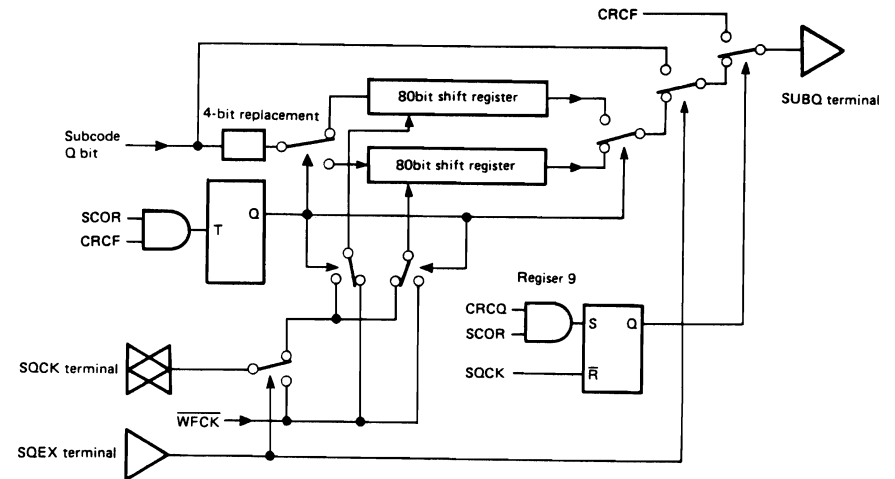
*5 : CRCF when CRCQ flag is "1", undefined when "0".

SQEX= "L" level



*6 : CRCF when CRCQ flag is "1", Q98, Q1 when "0".

(2) Timing chart of sub code outputs



CIRCUIT DESCRIPTION

● **EFM demodulation**

1) Playback of bit clock by EFM-PLL circuit

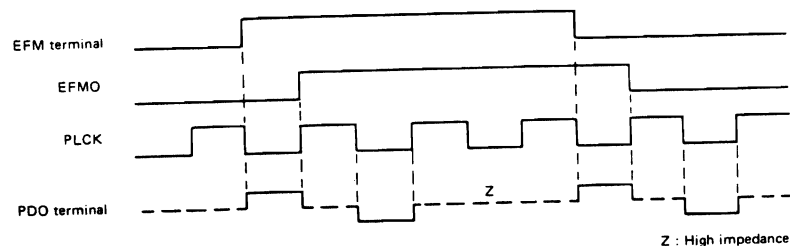
The EFM signal read out of the optical block contains a clock component of 2.16MHz. Therefore, it is possible to take out a bit clock (PLCK) of 4.32MHz synchronized with this clock by the EFM-PLL circuit.

At each edge of EFM signal, phase comparison is made with PLCK, which is 1/2 of VCO, is made and output is

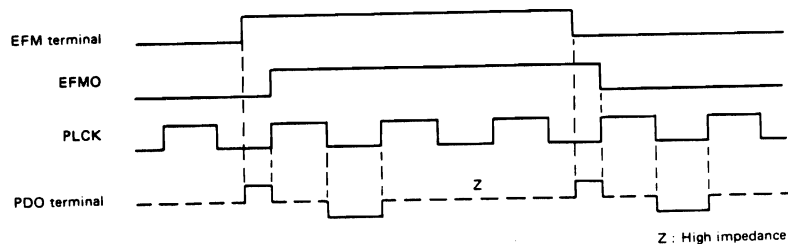
made by TRI STATE out of PDO terminal. The mean value of PDO terminal is about 1/2 VDD if synchronized, but the mean value drops when VCO becomes higher. On the other hand, the mean value increases when VCO becomes less.

The timing charts of EFM terminal, EFMO, PLCK and PDO are shown in Fig. 6-7.

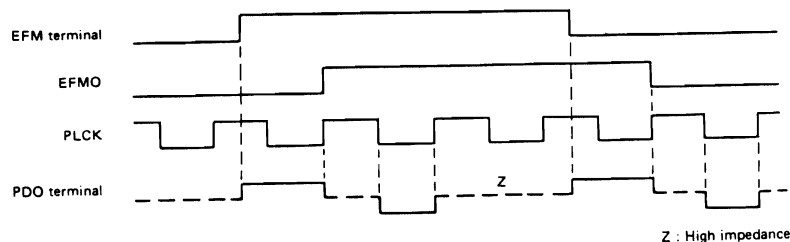
(a) When EFM signal and VCO are synchronized



(b) When VCO is higher than EFM signal



(c) When VCO is less than EFM signal



Timing charts of EFM-PLL circuit

CIRCUIT DESCRIPTION

2) Detection, protection and interpolation of frame synchronizing signals

There are cases during recording where the same pattern is detected in the data due to the influence of drop-out and jitter, even if a pattern that is same as the synchronizing signal will not appear.

On the other hand, there also are cases where original frame synchronizing signal is not detected. Therefore, protection and interpolation are required besides detection.

The edge portion only of EFM signal (EFMO) latched with PLCK is converted to "1" and the rest to "0", and then input is to a 23 bit shift register and a frame synchronizing signal is detected.

In order to protect a frame synchronizing signal, a window is provided and the same patterns outside of this window are removed. This width can be selected with WSEL. If no frame synchronizing signal is located in this window, interpolation is made with a signal produced by 588-mal counter ($4.3218\text{MHz}/588 = 7.35\text{kHz}$)

A 4 bit counter for counting the number of these frames to be interpolated is provided, and when its count reaches the level selected with GSEL, GSEM, the window is ignored and the 4 bit counter is reset with the next frame synchronizing signal. the GTOP terminal is of "H" while this operation is performed. Further, GFS terminal is of "H" when the frame synchronizing signal generated by the 588-mal counter for making interpolation is synchronized with the frame synchronizing signal from the disc.

The frame synchronizing signal before passage through the window or the window is output out of UGFS (DA05 terminal at the time when PSSL = L.)

WSEL	Window width
0	±3 clock
1	±7 clock

GSEM	GSEL	Number of frames to be interpolated	UGFS (PSSL = "L")
0	0	2 frames	Window
0	1	4 frames	Window
1	0	8 frames	Frame synchronizing signal before passage through window.
1	1	13 frames	Window

The timing for write request signal (WREQ), Write Frame Clock (WFCK), etc. is generated based on the protected and interpolated frame synchronizing signal.

3) EFM demodulation

14 bit data is taken out of the 23 bit shift register and is demodulated to 8 bit data through 14 → 8 conversion circuit composed of array logics. Then a write request (WREQ) signal is output to the RAM interface block, and the data is then output to the data bus (DB08~DB01) terminals) of the RAM in accordance with the OENB signal transmitted from said block.

● **Sub code demodulation**

1) Sub code demodulation

synchronizing signals S0, S1 of 14 bit sub codes are detected out of the 23 bit shift register, and sampling is made in the timing that is synchronized with WFCK.

After delay of S0 by one frame, S0 + S1 is output out of SCOR terminal and S0 - S1 is output out of SBSO terminal (only when SCOR = H.)

Data (P~W) of sub codes only is input to the register in the timing synchronized with WFCK after EFM demodulation; and sub code Q is output out of SUBQ terminal, and at the same time, it is loaded in the 8 bit shift register and is output out of SBSO terminal in correspondence to a clock from EXCK terminal.

The details of this timing will be shown in the paragraph of CPU interface.

2) Sub code Q error detection

The CRC sub code result is output from the CRCF pin in synchronism with the SCOR pin. It goes "L" when an error is detected. At the same time as the CRCQ flag is "1", the CRCF flag is output from the SUBQ pin during the time from the rising edge of the SCOR pin to the trailing edge of the SUBQ pin. This timing is detailed in "CPU interface".

CIRCUIT DESCRIPTION

● **RAM interface (generation of external RAM address)**

1) Request from EFM demodulation block (Write RAM request)

When one symbol of demodulation is complete in the EFM demodulation block, the EFM demodulation block requests to write data to the external RAM to the RAM interface block. This request is WREQ signal. This block gives priority orders to requests from other blocks and processes these requests.

When EFM write request is received, an address is generated to the RAM and Write Enable state is produced. Furthermore, a data output instruction is issued against the EFM demodulation block. This instruction is OENB signal.

Clocks of PLL system are used for EFM block and for requests (WREQ) from EFM block, but clocks of X'Tal system are used for processing thereafter.

2) Request from D/A converter output circuit (Read to D/A request)

This is a de-interleaved data request issued out of the timing generator in this block. This request is of the highest priority among all requests, and addresses of three types are generated against this request.

This request is generated once every 24 periods based on the period of system clock C212 (8.4672MHz/4). The data output out of the RAM is C2 pointer first, less significant 8 bits out of 16 bits and finally more significant 8 bits.

3) Request from error correction block (C1/C2 correction, pointer R/W)

The error correction block requests the data located on the system (C1/C2) to be corrected. Furthermore, there is a request to rewrite incorrect data to correct data. In addition, there is a request for pointer R/W which indicates reliability of data.

These requests are made by the 8 bit data directed to the RAM interface block from the error correction block. The requests from the error correction unit are of the lowest priority among requests of three types. After acceptance of a request, data from RAM is directed to the 3rd clock of C212.

The data of acceptance of a request is output to the error correction block as a PREN signal. This block generates the address of the requested data, and controls R/W of the RAM at the same time.

4) Address generation

The data after EFM demodulation is data subjected to interleave processing. This interleave processing is subjected to data lag by the unit of a frame. Data of 108 frames are required for de-interleave. In other words, for obtaining one frame of audio data played in a certain length of time, data of 108 frames after EFM demodulation are required. Further, the system data of C1/C2 is of the system in the process of application of interleave, and therefore, is included in 108 frames.

Data in practice are generated continuously. That is, de-interleave should be updated by the unit of a frame. Therefore, Read/Write base counters are required. This base counter performs counting by the unit of a frame.

The writer base counter is used only at the time of EFM data writer. The address directed to the external RAM is determined by the relative lag value to EFM demodulation data and their number of frames.

5) Priority of address generation request

The system control block determines priority of address generation requests made to the RAM interface block.

The priority order is as follows beginning with higher priority.

1. Read to D/A request
2. Write to RAM request
3. C1/C2 request

The number of times of requests is as follows.

1. Requests of 12 times in the frame section
The number of times of address generation to it is 36 times.
2. Requests of 32 times in the frame section
The number of times of address generation to it is 32 times.
3. Maximum number of times of request (C1 Double error correction, C2 pointer copy)
Read R/W 64 times, Pointe R/W 65 times in one frame section
The number of times of address generation to it is 129 times.

288 C212 (clocks) are included in a frame, and the number of times of operation of the RAM in it is 197 times at maximum. In the system control block, against request 1, the timing of its occurrence is reserved in advance. Requests 2, 3 are not accepted in this timing. When requests 2, 3 are generated simultaneously, priority is given to request 2, and if a request is generated during execution of either request, priority is given to the job in execution.

6) Jitter margin

The EFM demodulation data is synchronized with data's playback system (PLL) as described earlier. Accordingly, it includes disturbance (wow, flutter, etc.) of disc rotation servo, etc. It is loaded to the external RAM. As the data taken out of the RAM is synchronized with the clock of X'Tal system, this RAM is subjected to time axis correction.

However, the limit of time axis correction is determined by the capacity of the RAM. In this system, other data is destroyed when read/write frames are spaced apart by ± 5 frames. In such a status how the playback sound is cannot be guaranteed. The base counter monitor is provided in order to avoid it.

In other words, when the difference between read base counter and write base counter exceeds ± 4 frames, the write base counter is set in the value of the read base counter. As a result, there is no case where data without error correction is output to the D/A.

The RAOV signal is of "H" for one frame (WFCK) section when the difference between base counters exceeded ± 4 frames.

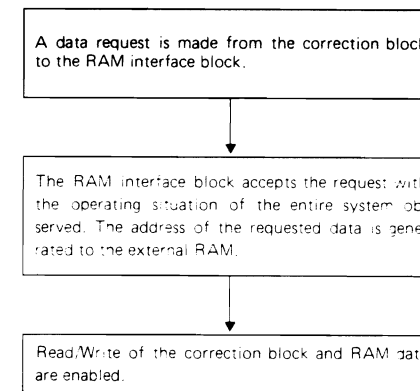
● **Error correction**

- 1) The error correction block makes correction up to double errors with each of C1 correction and C2 correction.
- 2) This system adopts a unique pointer erasure method in order to minimize erroneous correction. Accordingly, the external 16k RAM stores these pointer data in addition to audio data.
- 3) The pointer generated in C1 correction is called C1 pointer and the pointer generated in C2 correction is called C2 pointer.
- 4) When the data of C1 system is judged as reliable, a C1 pointer is set in this system.
- 5) During C2 correction, whether correction is to be made or not to be made and whether the data is reliable or unreliable are judged from the error location, locations and number of C1 pointers obtained through computation. A C2 pointer is set against an unreliable word (16 bits).
- 6) The word in which a C2 pointer was set is subjected to previous value hold or mean value interpolation when it is output out of this LSI.
- 7) Terminal C2FL becomes "H" when one or more C1 pointers are set in the data included in the C2 system at the time of C2 correction. C2FL is reset to "L" when a period of minimum 472ns after deactivation of terminal RFCK. C2FL is the AND of C2F1 and C2F2.

Note : 472ns : One period of 2.1168MHz

CIRCUIT DESCRIPTION

8) The flow of data with the external RAM is as follows.



9) When PSSL is set at "L", a signal that is capable of monitoring error correction is output. C1F1, C1F2, C2F2 output to DA01~DA04 are these monitor signals. This signal is reset to "L" when a period of minimum 472 ns has elapsed since deactivation of RFCK.

The levels and meanings of these signals at the time of deactivation of RFCK are as follows.

C1F1	C1F2	C1 correction status
0	0	No Error
1	0	Single error correction
0	1	Double error correction
1	1	Irretrievable error

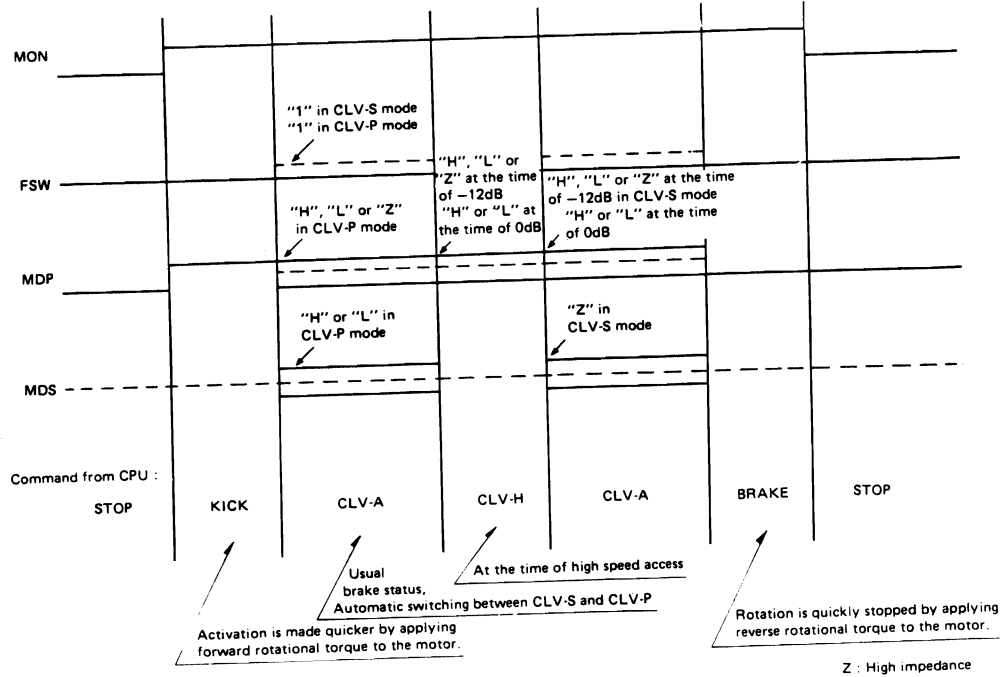
C2F1	C2F2	C2FL	C2 correction status
0	0	0	No Error
1	0	0	Single error correction
0	1	0	Double error correction
1	1	1	Irretrievable error

CIRCUIT DESCRIPTION

● **CLV servo control**

The spindle motor revolution is controlled with one selected out of the following seven modes in accordance with a command from the CPU. CLV is the abbreviation of Constant Linear Velocity. The output is composed of MDP terminal for controlling synchronization of velocity and phase, MDS terminal for controlling synchronization of velocity, FSW terminal for making selection of filter constant and MON terminal for controlling motor ON/OFF.

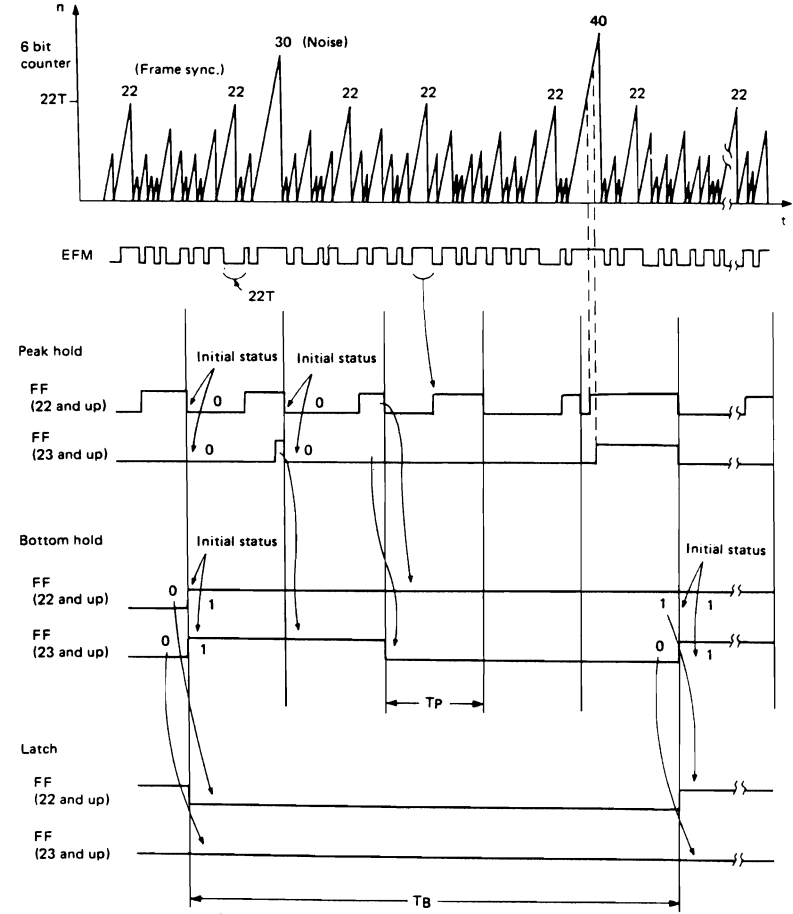
- 1) STOP : Register E = 0000'B (B means binary)
Mode for stopping the spindle motor.
MDP = FSW = MON = "L", MDS = "Z"
- 2) KICK : Register E = 1000'B
Mode for running the spindle motor in forward direction.
MDP = MON = "H", MDS = "Z", FSW = "L".
- 3) BRAKE : Register E = 1010'B
Mode for running the spindle motor in reverse direction.
MDP = FSW = "L", MDS = "Z", MON = "H".



Typical control of spindle motor

CIRCUIT DESCRIPTION

TP : RFCK/2 or RFCK/4 in the case of CLV-S, F8M/256 in the case of CLV-H
TB : RFCK/16 or RFCK/32 in the case of CLV-S, CLV-H



Timing chart in CLV-S, CLV-H mode (2)

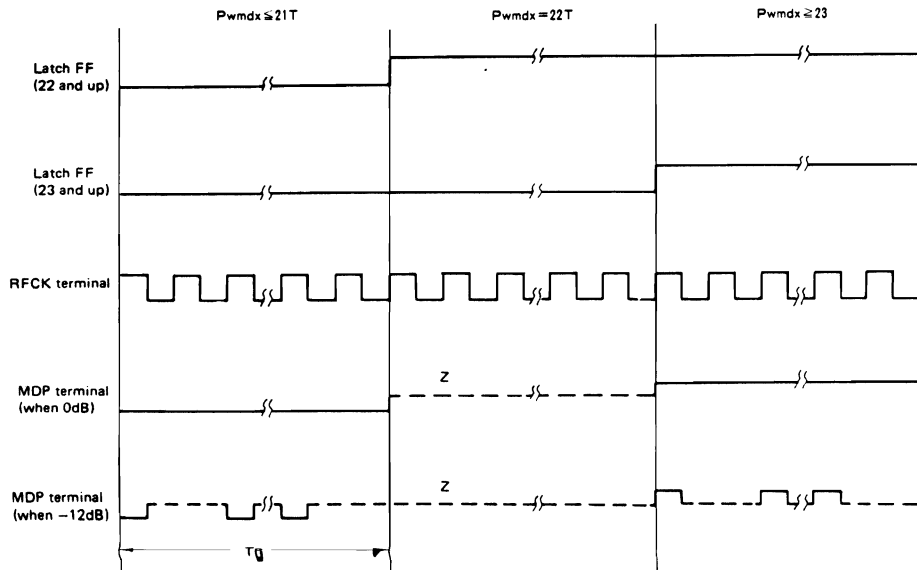
CIRCUIT DESCRIPTION

4) CLV-S : Register E = 1100'B

Rough servo mode used at the time of start of rotation, at the time of track jump and also when the EFM-PLL circuit is unlocked due to another reason. When the period of VCO's oscillation frequency 8.6436MHz is expressed as "T", the pulse width of a frame synchronizing signal is "22T" during specified revolution, and it is the maximum pulse width in a period of RFCK. In practice, however, there are pulses having widths over "22T" due to drop-off of EFM signal due to other reasons, and the frame synchronizing signal cannot be correctly detected unless such pulses are removed. Therefore, the maximum value (peak) of the pulse width of EFM signal is detected (called peak hold) in the period of RFCK/2 or RFCK/4, than the minimum value in this peak is detected (called bottom hold) in the period of RFCK/16 or RFCK/32, and this value is used as the frame synchronizing signal. "L" is produced out of MDS terminal while the frame synchronizing signal is "21T" or less, "Z" when it is "22T", or "H" when it is "23T" or more. Either 0dB or 12dB can be selected as its gain. MDS = "Z", FSW = "L", MON = "H".

5) CLV-P: Register E = 1111'B

PLL servo mode. When the NCLV of register 9 is "0", the phase of the WFCK/4 signal and the phase of the RFCK/4 signal are compared and output to the MDP pin. When NCLV = "1", 1/4 of the base counter frame frequencies at the Write side and the Read side are phase-compared and output to the MDP pin. It goes "H" when WFCK is slow, "L" when it is fast, and is "Z" when synchronized. If the 8.4672/2MHz period is T, and the time when WFCK is "H" is tHW, then the MDS pin outputs a signal which goes "H" during the time from the trailing edge of WFCK to the time represented by (tHW-279T) X 32, and then goes "L" until the next trailing edge of WFCK. MDS = "H" when tHW = 279T, MDS = "L" when tHW ≥ 279T. The MDS pin varies between 32T and 544T, in 32T steps, when 280T ≤ tHW ≤ 296T. For example, when synchronized (rotating at the standard speed), that is when tHW = 288T, a 7.35kHz signal, with a duty cycle of 50% is output. FSW = "Z", MON = "H".



Timing chart in CLV-S, CLV-H mode (1)

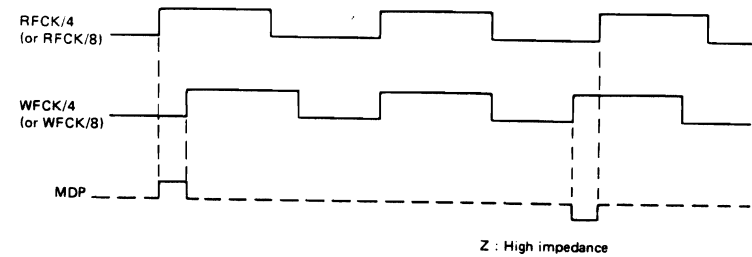
CIRCUIT DESCRIPTION

6) CLV-P: Register E = 1111'B
PLL servo mode.

Phase comparison of signals WFCK/4 and RFCK/4 or WFCK/8 and RFCK/8 is made, and output is made out of MDP terminal. "H" when WFCK has delayed, "L" when WFCK is fast, and "Z" when synchronized. When the period of 8.4672/2MHz is expressed at T and the length of time when WFCK is "H" is expressed at tHW, such a signal that is of "H" during (tHW-279T)

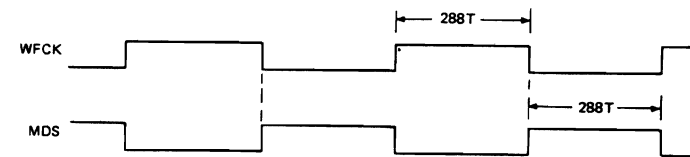
x 32 with 7.35kHz as a period and that is "L" during the remaining time is produced out of MDS terminal. MDS = "L" when tHW ≤ 279T, MDS = "H" when tHW ≤ 297T. When 280T ≤ tHW ≤ 296T, the MDS terminal changes in 32T steps from 32T to 544T. When synchronized, for instance, that is, when tHW = 288T, a signal of 7.35kHz of DUTY 50% is produced. FSW = "Z", MON = "H".

MDP terminal

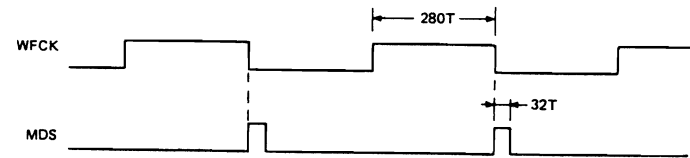


MDS terminal (The Period of 4.2336MHz is expressed as "T".)

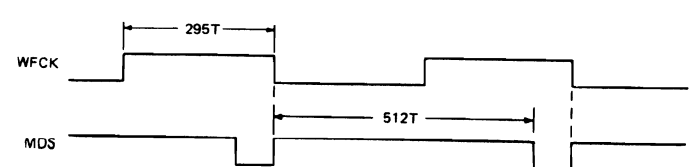
(1) When rotating at specified velocity



(2) When rotation becomes fast



(3) When rotation becomes slow



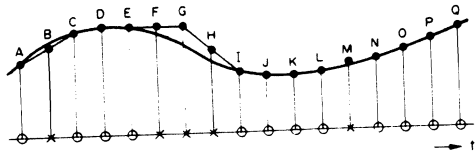
Timing chart in CLV-P mode

CIRCUIT DESCRIPTION

7) CLV-A: Register E = 0110'B
 The mode used for normal play status. The GFS signal ("H" when locked, "L" when unlocked), after frame sync detection, protection and insertion block, is sampled at WFCK/16, and functions in CLV-P mode when the signal is "H". When the "L" signal continues for 8 times, the mode is automatically changed to CLV-S mode. When in the CLV-S mode, setting of the peak hold period, and setting of the period and gain of the bottom hold of the CLV-S and CLV-H are performed in register D, and the selection of each mode is performed in register E. The description of these registers are detailed in "CPU interface".
Note: When PSSL = "L", DA07 pin outputs WFCK/4 or WFCK/8 as FCKV, and DA08 outputs EFCK/4 or EFCK/8 as FCKX.

● Interpolation and D/A converter interface
 1) Interpolation circuit block

3 byte data can be obtained with a Read to D/A request. They are C2 pointer, less significant 8 bits and more significant 8 bits. The total 16 bits constitute the data generated per sampling (2's complement).
 The C2 pointer expresses the reliability of this 16 bit data. Therefore, data with C2 pointer is subject to interpolation in this block.



O : Without C2 pointer
 X : With C2 pointer

Mean value interpolation

$$B = \frac{1}{2} (A + C)$$

$$H = \frac{1}{2} (E + I) \quad \text{: When pointers are continuous}$$

$$M = \frac{1}{2} (L + N)$$

Previous value hold

$$F = G = E$$

8) CLV-A' : Register E = 0101'B
 New auto servo mode added to the CX23035. The difference between CLV-A and CLV-A' is in the rough servo system. With the old rough servo system, the EFM pattern is measured by a crystal and the servo is applied so that the width of the sync pattern is a fixed value, and the rotation speed of the spindle motor is roughly fixed. In this case, if the value is out of the VCO capture range, the VCO never locks with the EFM. With the new rough servo system, a VCO is used for measurement instead of a crystal. If the VCO center is shifted from true center the VCO tends to lock, since the rotation of the spindle motor varies in the same direction.
 The new rough servo functions only in CLV-A' mode. The rough servo in CLV-A mode and CLV-S mode is the old rough servo.

16 bit data is alternately output to L-ch and R-ch. R-ch data is output in the section in which LRCK is "L" and L-ch data is output in the section in which LRCK is "H". C2PO signal outputs C2 pointer to the 16 bit data directed to DA01-DA16 (PSSL = H), DA16 (PSSL = L). In other words, it means that the 16 bit data that is output when C2PO is "H" is interpolated data.

2) Explanation of muting and attenuator

In the muting block it is possible to mute (-∞ dB) or attenuate (-12dB) the audio signal in accordance with the MUTG terminal and ATTM signal of the CPU interface block.

ATTM	MUTG	Attenuation value	Remarks
0	0	0dB	
1	0	-12dB	
0	1	-∞ dB	See Note
1	1	-12dB	See Note

NOTE : When the MUTG is set to "H" level with the NCLV flag set to "0", the read base counter value is continuously loaded into the write base counter as well as the muting.
 Except at CLV-A, CLV-P, CLV-S, or CLV-A' with the NCLV flag set to "1", the base counter is loaded.

CIRCUIT DESCRIPTION

● Mode setting

The various kinds of mode can be set by combining the following pins. (Refer to the table below.)

MD1 pin : Mainly for selection of the oscillator clock at the XTAI or XTAO pin.

MD2 pin : Mainly for selection of the digital out function.

MD3 pin : Mainly for selection of the digital filter function.

PSSL pin : Mainly for selection between serial and parallel output.

SLOB pin : Selection between offset binary and 2's complement.

Input terminal						Function				(Note)	Compatible IC	
MD1	MD2	MD3	PSSL	SLOB	8M/16M	DO OFF/ON	DF OFF/ON	P/S	OB/2's	GD ROM/AUDIO	CXD1125	CXD1130
L	L	L	L	L	16M	DO ON	DF ON	Ser	2's	AUDIO		
L	L	L	H	H	↓	↓	↓	Para	OB	↓		
L	L	H	L	L	↓	↓	DF OFF	Ser	2's	↓	○	
L	H	L	L	L	↓	DO OFF	DF ON	↓	↓	↓		○
L	H	L	H	H	↓	↓	↓	Para	OB	↓		○
L	H	H	L	L	↓	↓	DF OFF	Ser	2's	↓		○
L	H	H	H	H	↓	↓	↓	Para	OB	↓		○
H	L	L	L	L	8M	↓	DF ON	Ser	2's	↓		○
H	L	L	H	H	↓	↓	↓	Para	OB	↓		○
H	L	H	L	L	↓	↓	DF OFF	Ser	2's	↓		○
H	L	H	H	H	↓	↓	↓	Para	OB	↓		○
H	H	H	L	L	16M	DO ON	↓	Ser	2's	GD ROM		○
H	H	H	H	L	8M	DO OFF	↓	↓	↓	↓	○	○

(Note)

- 8M/16M : Selection of clock, XTAL or XTAO. 8.4672MHz/16.9344MHz
- DO OFF/ON : Digital out OFF/ON
- DF OFF/ON : Digital filter OFF/ON

- P/S : Parallel output/serial output
- OB/2's : Offset binary/2's complement
- CD ROM/AUDIO : Compatible to CD ROM/Compatible to audio

1) Selection of clock

The oscillator clock for XTAI and XTAO is available at 16.9344MHz and 8.4672MHz. However, when digital out is used, the clock must be set to 16.9344MHz.

2) Selection of digital out (Refer to "D/A interface")

When digital out is set to ON, a signal conforming to the D/A interface format is output from the DOTX pin. When it is set to OFF, the DCTX pin outputs the WFCK signal. In the DP-969, this function is fixed to ON.

3) Selection of digital filter

When the digital filter function is set to ON, the DAC interface signal are all set to double speed.

4) Selection of parallel output/serial output

When the parallel output is selected, DA01 to DA16 pins output the 16-bit parallel data. When the serial output is selected, DA01 to DA16 pin output the following signals respectively.

- DA01 → C1F1 : Error correction status monitor
- DA02 → C1F2 : output at C1 decode.
- DA03 → C2F1 : Error correction status monitor
- DA04 → C2F2 : output at C2 decode.
- DA05 → C2FL : Correction status output,
C2FL = C2F1-C2F2.

DA06 → C2PO : C2 pointer signal.

DA07 → RFCK : Read frame clock signal, 7.35kHz when locked to the crystal line.

DA08 → WFCK : Write frame clock signal, 7.35kHz when locked.

DA09 → PLCK : 1/2 of the divided signal from the VCO pin, 4.3218MHz when locked.

DA10 → UGFS : Non-protect frame sync signal.

DA11 → GTOP : Frame sync protect status display signal.

DA12 → RAOV : Jitter margin over or underflow display signal.

DA13 → C4LR : 4 times the LRCK signal.

DA14 → C2T0 : Bit clock (invert signal of C2T0).

DA15 → C2T0 : Internal system clock (4.2336MHz when DF is ON, 2.1168MHz when CXD1125Q or DF is OFF).

DA16 → DATA : Serial data output (MSB or LSB first output).

CIRCUIT DESCRIPTION

5) Selection of OFFSET BINARY/2'S COMPLEMENT

When the SLOB pin is "H", an offset binary signal is output, and when it is "L", a 2's complement signal is output.

6) Selection of CD ROM/AUDIO compatibility

When MD1 = MD2 = MD3 = "H", the player is compatible with a CD ROM and outputs the C2 pointer for each byte. At the same time, the average value interpolation and the previous value holding operations are not performed. For example, when there is an error in the upper 8 bits of the 16 bits, only the C2 pointer corresponding to the upper 8 bits goes "H", and the lower 8 bits are processed as the correct data.

• D/A Interface

The player incorporates a D/A interface output (digital output) and the digital signal is output from the DOTX pin. The digital signal is output after passing through interpolation, mute and attenuator circuits. The 4 control bits (ID0, ID1, COPY, EMPHASIS) in the C-bit channel status perform a CRC check and are revised only when it's OK.

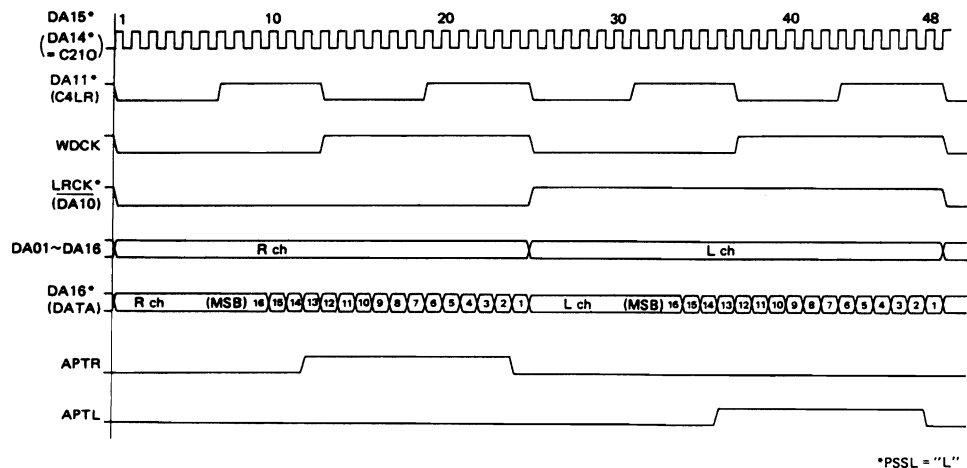
• Countermeasures to defect

To counter a defect, the PDC pin is set to "Hi-Z" during the time until GFS goes "H" again after inverting from "H" to "L" or after approx. 0.55ms has elapsed. However, this operation is performed only when the HZPD flag of register 9 is "1". When HZPD = "0", it will never be set to "Hi-Z".

The signal switching between the rough servo in the CLV-A or CLV-A' mode and the PLL servo is output from the LOCK pin. After the GFS signal is sampled at WFCK/16, and when the signal is "1", the LOCK pin goes "H", when a "0" is present 8 times in a row, the LOCK pin goes "L".

This operation is similar to that for the FSW pin. However, while the FSW outputs a fixed signal when not in CLV-A' mode, the LOCK pin always output the above signal.

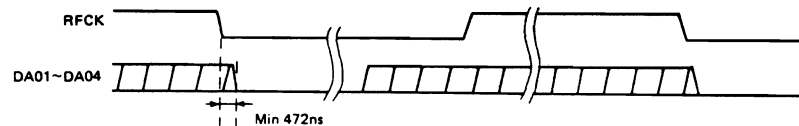
• Timing chart



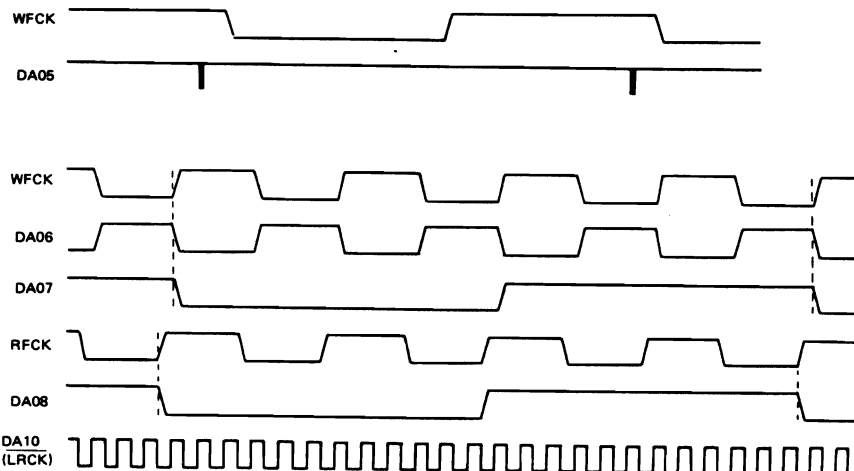
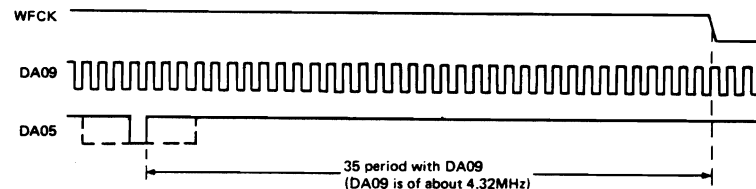
Timing chart of audio output

*PSSL = "L"

CIRCUIT DESCRIPTION

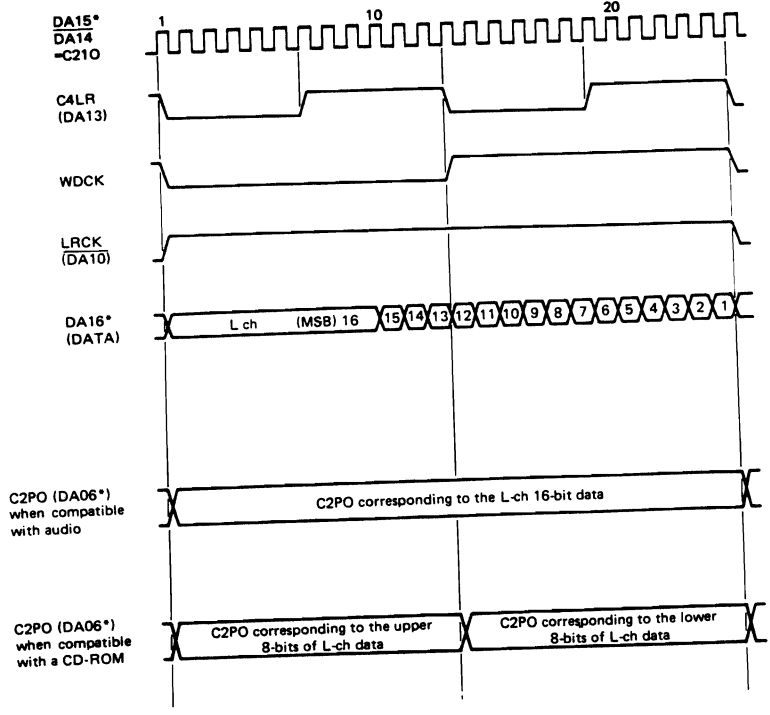


- DA01 ~ DA04 (C1F1, C1F2, C2F1, C2F2) are cleared when a period of minimum 472 ns has elapsed since RFCK was reactivated.
- ANDing signal of C2F1 and C2F2 is output out of C2FL terminal.



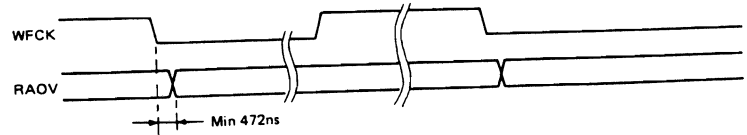
Timing chart of DA01 ~ DA16 output when PSSL = "L"

CIRCUIT DESCRIPTION



Timing chart of C2PO output (when PSSL="L")

* RAOV becomes "H" for one frame (synchronized with WFCK) when a jitter that exceeds ±4 frames is generated between RFCK and WFCK.

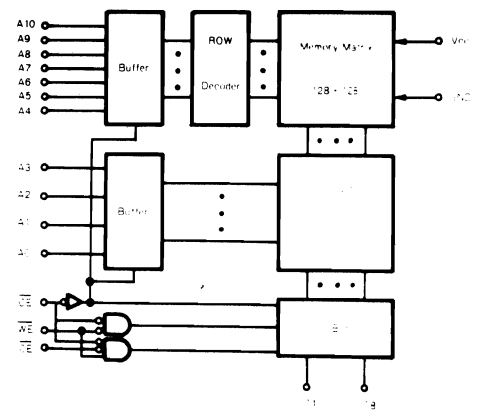


Timing chart of RAOV output

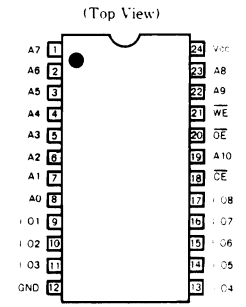
CIRCUIT DESCRIPTION

Static RAM CXK5816SP-12L
(X32-1170-00 : IC7)

Block Diagram



Terminal connection diagram



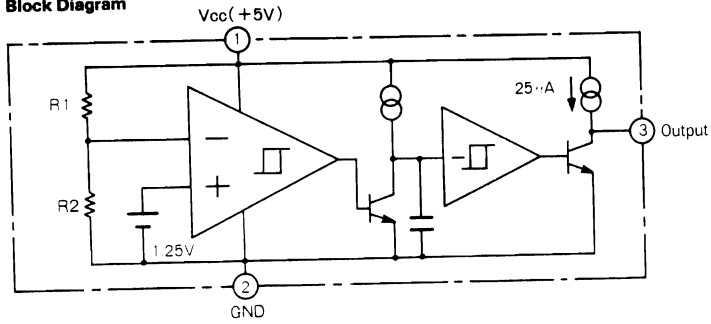
Explanation of terminals

Terminal name	Function
A0 ~ A10	Address input
I/O1 ~ I/O8	Data input/output
CE	Chip enable input
WE	Write enable input
OE	Output enable input
Vcc	+5V
END	Ground

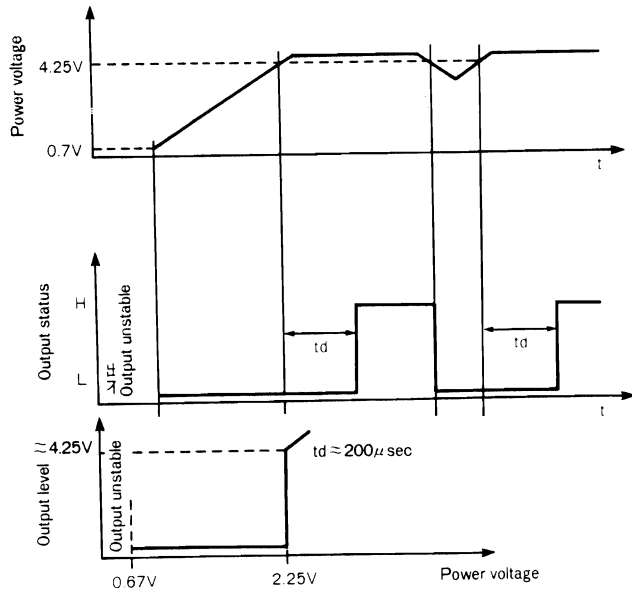
CIRCUIT DESCRIPTION

Reset IC: M51951ASL (X32-1170-00: IC11)

Block Diagram



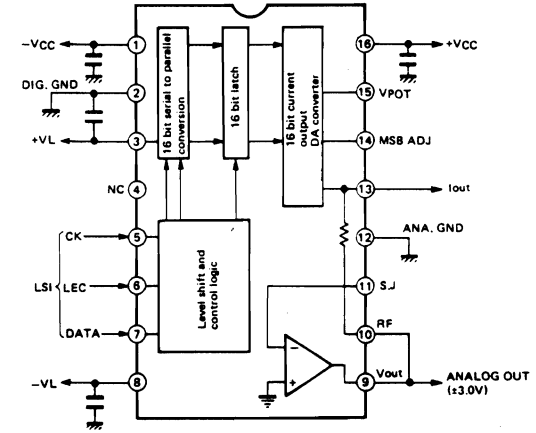
Operating Waveform



CIRCUIT DESCRIPTION

DA Converter: PCM56P-K
(X25-3050-00: IC1, IC2)

Block diagram/
Terminal connection diagram

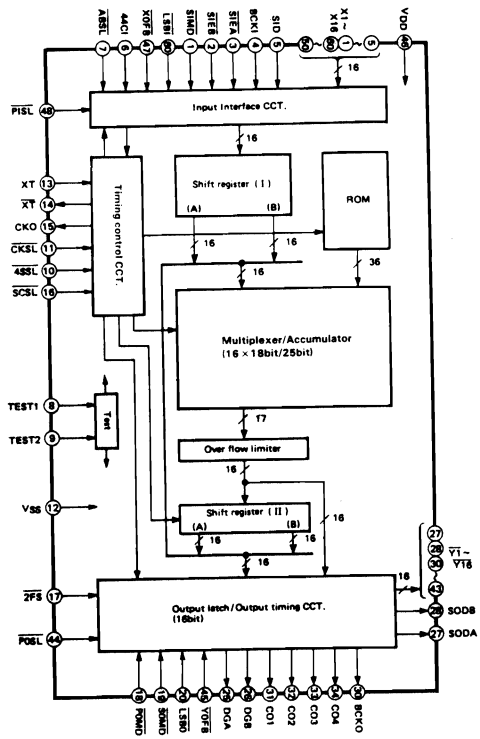


Explanation of terminals

Terminal No.	Terminal name	Function	Terminal No.	Terminal name	Function
1	-Vcc	Analog negative power supply.	9	Vout	Voltage output
2	DIG. GND	Digital ground.	10	RF	Feedback resistor.
3	+VL	Logic positive power supply.	11	S.J	Summing junction (op amp. input).
4	NC	No connection.	12	ANA. GND	Analog ground.
5	CK	Clock input.	13	Iout	Current output.
6	LEC	Latch enable control input.	14	MSB ADJ	MSB adjustment terminal.
7	DATA	Data input.	15	V. POT	Potentiometer terminal.
8	-VL	Logic negative power supply	16	+ Vcc	Analog positive power supply.

CIRCUIT DESCRIPTION

Digital filter: SM5804D
(X25-3050-00: IC14)
Block diagram



CIRCUIT DESCRIPTION

Explanation of Pins

With this LSI, the switching between the serial and parallel inputs/outputs is performed by the PISL and POSL pins. Some

of the functions of pins X1 to X16 and Y1 to Y16 may be changed by this switching.

All the terminals of this unit function with PISL = H.

Note: ip designates an input jack with a pull-up resistor.

Pin No.	PISL = H		PISL = L		Function
	Pin Name	I/O	Pin Name	I/O	
1	SIMD	ip	X5	ip	Serial input mode switching
	SIEB	ip	X4	ip	Parallel data input (Bit 5)
2	SIEA	ip	X3	ip	B CH serial input enable
	BCKI	ip	X2	ip	A CH serial input enable
3	SID	ip	X1	ip	Parallel data input (Bit 3)
	44C	ip	←	ip	Serial input bit clock input
4	ABSL	ip	←	ip	Parallel data input (Bit 2)
	TEST 1	ip	←	ip	Serial input data
5	TEST 2	ip	←	ip	Parallel data input (LSB)
	4SSL	ip	←	ip	44.1 kHz sync clock input
6	CKSL	ip	←	ip	ABSL = H → 44 CI clock, H/L = A CH/B CH ABSL = L → 44 CI clock, H/L = B CH/A CH
	Vss	←	←	←	Test input 1 (Normally Open)
7	2FS	ip	←	ip	Test input 2 (Normally Open)
	PGBL	ip	←	ip	Normally 4SSL = H or Open 4SSL = L when input is 16.9344 MHz or 17.2872 MHz
8	X1	ip	←	ip	CKSL = H → External clock input CKSL = L → X'tal oscillation
	X2	ip	←	ip	GND power supply pin (0 V)
9	X3	ip	←	ip	CKSL = H → Clock input CKSL = L → X'tal oscillation input.
	X4	ip	←	ip	CKSL = H → (Open) CKSL = L → X'tal oscillation output.
10	X5	ip	←	ip	Clock output
	X6	ip	←	ip	System clock 96 fs → SCSS = H System clock 98 fs → SCSS = L
11	X7	ip	←	ip	Open
	X8	ip	←	ip	POMD = H → Normal parallel output mode. POMD = L → In-phase parallel output mode.
12	X9	ip	←	ip	SOMD = L with serial output.
	X10	ip	←	ip	LSBO = H → MSB-first serial output LSBO = L → LSB-first serial output
13	X11	ip	←	ip	(INC)
	X12	ip	←	ip	(INC)
14	X13	ip	←	ip	(INC)
	X14	ip	←	ip	(INC)
15	X15	ip	←	ip	(INC)
	X16	ip	←	ip	(INC)
16	X17	ip	←	ip	DGA A CH deglitch control output.
	X18	ip	←	ip	DGB B CH deglitch control output.
17	X19	ip	←	ip	SODA A CH serial data output.
	X20	ip	←	ip	Parallel output (inverted, LSB)

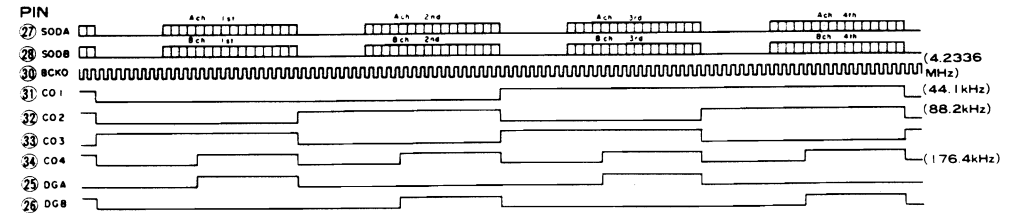
CIRCUIT DESCRIPTION

Pin No.	PISL = H		PISL = L		Function
	Pin Name	I/O	Pin Name	I/O	
28	SODB	O			B CH serial data output.
			$\overline{Y2}$	O	Parallel output (inverted, Bit 2).
29	(NC)				Internally short-circuited to V _{DD} . Not to be connected externally.
30	BCKO	O			Serial output bit clock output.
			$\overline{Y3}$	O	Parallel output (inverted, Bit 3).
31	CO1	O			Serial output control clock 1
			$\overline{Y4}$	O	Parallel output (inverted, Bit 4).
32	CO2	O			Serial output control clock 2
			$\overline{Y5}$	O	Parallel output (inverted, Bit 5).
33	CO3	O			Serial output control clock 3
			$\overline{Y6}$	O	Parallel output (inverted, Bit 6).
34	CO4	O			Serial output control clock 4.
			$\overline{Y7}$	O	Parallel output (inverted, Bit 7).
35	(NC)	Hz			(NC)
			$\overline{Y8}$	O	Parallel output (inverted, Bit 8).
36	(NC)	Hz			(NC)
			$\overline{Y9}$	O	Parallel output (inverted, Bit 9).
37	(NC)	Hz			(NC)
			$\overline{Y10}$	O	Parallel output (inverted, Bit 10).
38	(NC)	Hz			(NC)
			$\overline{Y11}$	O	Parallel output (inverted, Bit 11).
39	(NC)	Hz			(NC)
			$\overline{Y12}$	O	Parallel output (inverted, Bit 12).
40	(NC)	Hz			(NC)
			$\overline{Y13}$	O	Parallel output (inverted, Bit 13).
41	(NC)	Hz			(NC)
			$\overline{Y14}$	O	Parallel output (inverted, Bit 14).
42	(NC)	Hz			(NC)
			$\overline{Y15}$	O	Parallel output (inverted, Bit 15).
43	(NC)	Hz			(NC)
			$\overline{Y16}$	O	Parallel output (inverted, MSB).
44	POSL	ip		ip	POSL = H - Serial output system. POSL = L - Parallel output system.
45	YOFB	ip		ip	YOFB = H - 2's complement display output. YOFB = L - Offset binary display output.
46	V _{DD}				+ve power supply pin (5 V).
47	XOFB	ip		ip	XOFB = H - 2's complement display input. XOFB = L - Offset binary display input.
48	PISL	ip		ip	PISL = H - Serial input system. PISL = L - Parallel input system.
49	(NC)				(NC)

CIRCUIT DESCRIPTION

Pin No.	PISL = H		PISL = L		Function
	Pin Name	I/O	Pin Name	I/O	
50	(NC)	ip			(NC)
			X16	ip	Parallel data input (MSB).
51	(NC)	ip			(NC)
			X15	ip	Parallel data input (Bit 15)
52	(NC)	ip			(NC)
			X14	ip	Parallel data input (Bit 14)
53	(NC)	ip			(NC)
			X13	ip	Parallel data input (Bit 13)
54	(NC)	ip			(NC)
			X12	ip	Parallel data input (Bit 12)
55	(NC)	ip			(NC)
			X11	ip	Parallel data input (Bit 11)
56	(NC)	ip			(NC)
			X10	ip	Parallel data input (Bit 10)
57	(NC)	ip			(NC)
			X9	ip	Parallel data input (Bit 9)
58	(NC)	ip			(NC)
			X8	ip	Parallel data input (Bit 8)
59	(NC)	ip			(NC)
			X7	ip	Parallel data input (Bit 7)
60	LSBI	ip			LSBI = H - MSB-first serial input LSBI = L - LSB-first serial input.
			X6	ip	Parallel data input (Bit 6)

Serial Output Timing (S_{ODM} = L, S_{CSL} = H, system clock = 4.2336 MHz)

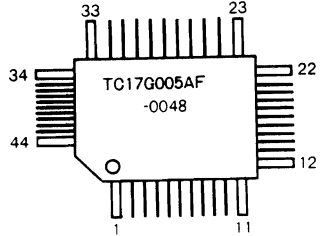


CIRCUIT DESCRIPTION

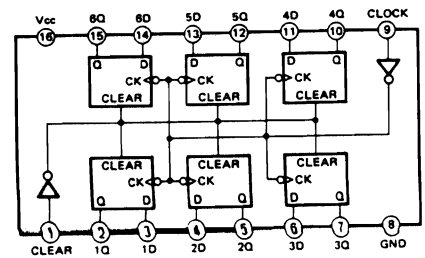
D/A distortion correct TC17G005AF-0048
(X25-3050-00: IC15)
Explanation of terminals

Terminal No.	Terminal name	I/O	Function
1	DLD	O	Lch data output
3	Lch	O	Lch D/A distortion correct output
4	V _{SS}	—	GND
5	BCKD	O	Clock output
7	LEP	O	Latch enable control output
8	V _{SS}	—	GND
9	Rch	O	Rch D/A distortion correct output
11	RPD	O	Rch data output
14	X ¹¹⁰	O	Crystal oscillator input terminal (16.934MHz)
15	X ¹¹¹	I	
17	V _{DD}	—	+5V
28	V _{SS}	—	GND
39	V _{DD}	—	+5V
40	LR	I	LRCK input (4fs)
41	BCK	I	BCK input (4fs)
42	DR	I	Rch data input
43	DL	I	Lch data input

Terminal connection diagram



Hexa D Flip-flop TC74HC174F
(X25-3040-00: IC2)
Block diagram

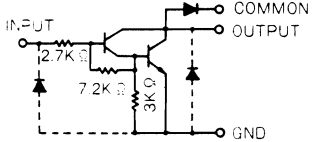
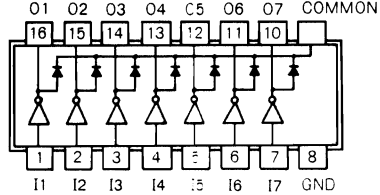


Truth table

Inputs			Outputs
Clear	Clock	D	Q
L	X	X	L
H	↑	H	H
H	↑	L	L
H	L	X	Q ₀

CIRCUIT DESCRIPTION

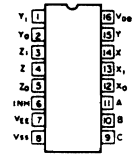
Transistor array (X25-3040-00: IC3)
TD62003AP DARLINGTON DRIVER
Pin configuration



μPD4053BC 2-channel analog switch IC
(X32-1170-00: IC2)

The μPD4053BC is a multiplexer composed of a level converter and analog SWs. The switches corresponding to the required channels are turned on according to the digital signal input to the control terminals.

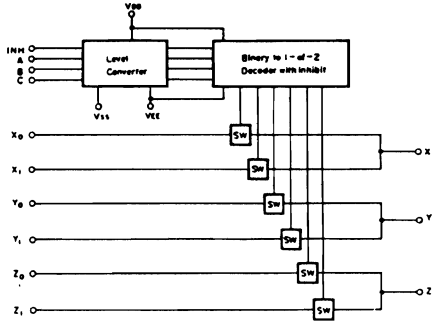
Block diagram



Truth table

INHIBIT	Control input			"ON" channel
	C*	B	A	
L	L	L	L	Z ₀ , Y ₀ , X ₀
L	L	L	H	Z ₁ , Y ₁ , X ₁
L	L	H	L	Z ₀ , Y ₁ , X ₀
L	L	H	H	Z ₁ , Y ₁ , X ₁
L	H	L	L	Z ₁ , Y ₀ , X ₀
L	H	L	H	Z ₁ , Y ₀ , X ₁
L	H	H	L	Z ₀ , Y ₁ , X ₀
L	H	H	H	Z ₁ , Y ₁ , X ₁
H	X	X	X	NONE

H: "H" level, L: "L" level, X: H or L



ADJUSTMENT

REGLAGE

No.	ITEM	INPUT SETTING	OUTPUT SETTING	PLAYER SETTING	ALIGNMENT POINT	ALIGN FOR	FIG
1	LASER POWER	-	Apply the sensor section of the optical power meter on the pickup lens.	Short-circuit pins TEST and turn power on to enter the Test mode. Press the REPEAT key, the tray opens and the LD emits light.	-	When the power is from 0.15 to 0.4mW, RF level is 1.0Vp-p or more, TE (servo open) is 2.0Vp-p or more and the diffraction grating is aligned correctly, the pickup is acceptable.	(a)
2	LASER PICKUP OPERATING CURRENT (Only when the pickup seems defective.)	-	Connect a DC ammeter across CN2 pin 6 and the pattern. (X32-1170)	Short-circuit pins TEST and turn power on to enter the Test mode. Press the REPEAT key, the tray opens and the LD emits light.	-	-5.5mA current value labeled on the laser pickup. If current is 40mA or more over the above value, it's defective.	(b)
3	VCO	-	Connect a frequency counter to CN11(PLCK) (X32-1170)	Turn Power OFF, then ON again. Stop mode	L9 (X32-1170)	4.27MHz	(c)
4	DIFFRACTION GRATING	Test disk Type 4	Connect an oscilloscope as follows. CH1: RF (X29-1870 Test pin) CH2: TE (X32-1170 pin 1)	Enter the test mode by turning Power ON while shorting the Test Pin. Press the CHECK key and confirm that the display is "0300".	-	Check that the diffraction grating is aligned correctly. (The grating cannot be adjusted.)	(d)
5	TRACKING ERROR BALANCE	Test disk Type 4	Connect an oscilloscope as follows. CH1: RF (X29-1870 Test pin) CH2: TE (X32-1170 pin 1)	Enter the test mode by turning Power ON while shorting the Test Pin. Press the CHECK key and confirm that the display is "0300".	TE BALANCE VR3 (X29-1870)	Symmetry between upper and lower patterns, or DC±0.05V	(e)
6	FOCUS ERROR BALANCE	Test disk Type 4	Connect an oscilloscope as follows. CH1: RF (X29-1870 Test pin) CH2: TE (X32-1170 pin 1)	Press the PLAY key, and confirm that the display is "0500".	FE BALANCE VR4 (X29-1870)	Optimum eye pattern	(f)
7	FOCUS GAIN	Test disc Type 4 Apply 900Hz, 40mVrms signal to CN3 pin 2 of PC board X32-1170	Use a servo jig, or connect a 47kΩ, 470pF LFP to pin 1 of CN3. (X32-1170)	Turn Power OFF then ON again, and press the PLAY key.	FOCUS GAIN VR1 (X29-1870)	40mVrms	(g)
8	TRACKING GAIN	Test disc Type 4 Apply 900Hz, 40mVrms signal to CN3 pin 4 of PC board X32-1170	Use a servo jig, or connect a 47kΩ, 470pF LFP to pin 5 of CN3. (X32-1170)	PLAY	TRACKING GAIN VR2 (X29-1870)	40mVrms	(g)
9	DAC OUTPUT	Test disk Type 4	Connect an AC voltmeter to the output terminal(FIXED).	Play the 1kHz, 0dB signal in track No.2.	VR1: L VR2: R (X25-3050)	1.9~2.0Vrms	(h)
10	DAC DISTORTION	Test disk Type 4	Connect an AC voltmeter to the output terminal(FIXED).	Play the 1kHz, -20dB signal in track No.15.	VR3: L VR4: R (X25-3050)	Minimum distortion	(h)
11	DAC DISTORTION	Test disk Type 4	Connect an AC voltmeter to the output terminal(FIXED).	Play the 100Hz, 0dB signal in track No.4.	VR5: L VR6: R (X25-3050)	Minimum distortion	(h)

(Note) Type 4 disk: SONY YEDS-18 Test Disk or equivalent.

N°	ITEM	REGLAGE D'ENTREE	REGLAGE DE SORTIE	REGLAGE DE LA LECTURE	POINT D'ALIGNEMENT	ALIGNEMENT POUR	FIG
1	PUISSANCE LASER	-	Appliquer la section détecteur du compteur de puissance optique sur la lentille du capteur.	Court-circuiter les broches TEST et mettre sous tension pour passer dans le mode d'essai. Appuyer sur la touche REPEAT, le plateau s'ouvre et le LD émet de la lumière.	-	Quand l'alimentation est de 0.15 à 0.4mW, le niveau RF de 1.0Vc-c ou plus, TE (asservissement ouvert) de 2.0Vc-c ou plus et le réseau de diffraction aligné correctement, le capteur est acceptable.	(a)
2	Courant de fonctionnement du capteur laser (Uniquement quand le capteur semble defectif.)	-	Raccorder un ampèremètre CC en travers de la broche 6 de CN2 et la forme. (X32-1170)	Court-circuiter les broches TEST et mettre sous tension pour passer dans le mode d'essai. Appuyer sur la touche REPEAT, le plateau s'ouvre et le LD émet de la lumière.	-	- 5.5mA de valeur de courant indiquée sur le capteur laser. Si le courant est de 40mA ou bien supérieur à la valeur ci-dessus, il est defectif.	(b)
3	VCO	-	Raccorder un compteur de fréquence à CN11(PLCK). (X32-1170)	Couper l'alimentation, puis la redonner. Mode d'arrêt	L9 (X32-1170)	4.27MHz	(c)
4	RESEAU DE DIFFRACTION	Disque test Type 4	Raccorder un oscilloscope comme suit. CH1: RF (X29-1870 broche test) CH2: TE (X32-1170 broche 1)	Entrer en mode de test en mettant l'alimentation en circuit tout en court-circuitant la broche test. Presser la touche CHECK et s'assurer que l'affichage est "0300".	-	Vérifier que le réseau de diffraction est correctement aligné. (Le réseau ne peut pas être ajusté.)	(d)
5	BALANCE D'ERREUR D'ALIGNEMENT	Disque test Type 4	Raccorder un oscilloscope comme suit. CH1: RF (X29-1870 broche test) CH2: TE (X32-1170 broche 1)	Entrer en mode de test en mettant l'alimentation en circuit tout en court-circuitant la broche test. Presser la touche CHECK et s'assurer que l'affichage est "0300".	TE BALANCE VR3 (X29-1870)	Symétrie entre les formes supérieure et inférieure ou DC=0.05V	(e)
6	BALANCE D'ERREUR DE MISE AU POINT	Disque test Type 4	Raccorder un oscilloscope comme suit. CH1: RF (X29-1870 broche test) CH2: TE (X32-1170 broche 1)	Presser la touche PLAY et s'assurer que l'affichage est "0500".	FE BALANCE VR4 (X29-1870)	Forme optimum	(f)
7	GAIN DE MISE AU POINT	Disque test Type 4 Appliquer un signal 900Hz, 40mVrms à la troche 2 de CN3 sur la plaquette X32-1170	Utiliser un gabarit d'asservissement ou raccorder un FPH de 47kΩ, 470pF la troche 1 de CN3.	Couper l'alimentation et la redonner puis presser la touch PLAY.	GAIN DE MISE AU POINT VR1 (X29-1870)	40mVrms	(g)
8	GAIN D'ALIGNEMENT	Disque test Type 4 Appliquer un signal 900Hz, 40mVrms à la troche 4 de CN3 sur la plaquette X32-1170	Utiliser un gabarit d'asservissement ou raccorder un FPH de 47kΩ, 470pF la troche 5 de CN3.	PLAY	GAIN D'ALIGNEMENT VR2 (X29-1870)	40mVrms	(g)
9	SORTIE DAC	Disque test Type 4	Raccorder un voltmètre CA sur la borne de sortie (FIXED).	Lire le signal 1kHz, 0dB dans la piste n° 2.	VR1: G VR2: D (X25-3050)	1.9~2.0Vrms	(h)
10	DISTORSION DAC	Disque test Type 4	Raccorder un voltmètre CA sur la borne de sortie (FIXED).	Lire le signal 1kHz, -20dB dans la piste n° 15.	VR3: G VR4: D (X25-3050)	Distortion minimum	(h)
11	DISTORTION DAC	Disque test Type 4	Raccorder un voltmètre CA sur la borne de sortie (FIXED).	Lire le signal 100Hz, 0dB dans la piste n° 4.	VR5: G VR6: D (X25-3050)	Distortion minimum	(h)

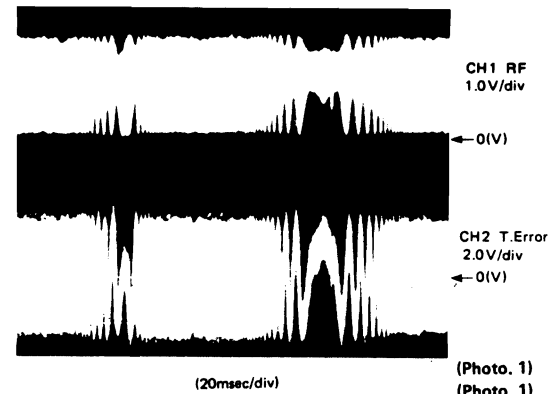
(Remarque) Disque de type 4: Disque test SONY YEDS-18 ou équivalent.

ABGLEICH

ADJUSTMENT/REGLAGE/ABGLEICH

NR.	GEGENSTAND	EINGANGS-EINSTELLUNG	AUSGANGS-EINSTELLUNG	SPIELER-EINSTELLUNG	ABGLEICH-PUNKT	ABGLEICHUNG	ABB
1	LASERLEISTUNG	-	Das Sensorteil des optischen Leistungsmeters auf die AufnahmeLinse ansetzen.	Die Stifte TEST kurzschließen und die Spannungsversorgung einschalten, um den Test-Modus zu aktivieren. Die Taste REPEAT drücken, dann öffnet sich der Trager, und die LD gibt Licht aus.	-	Venn bei einer Spannung von 0,15 bis 0,4 A der RF-Pegel 1,0V _s oder mehr, TE (Servo-Offen) 2,0V _s beträgt und das Beugungsgitter richtig ausgerichtet ist, ist der Abtaster in Ordnung.	(a)
2	BETRIEBSSTROM DES LASERTONABNEHMERS (Nur wenn der Tonabnehmer defekt zu sein scheint)	-	Ein-Gleichstrom-Apometer zwischen CN2 Stift 6 und dem Muster anschließen. (X32-1170)	Die Stifte TEST kurzschließen und die Spannungsversorgung einschalten, um den Test-Modus zu aktivieren. Die Taste REPEAT drücken, dann öffnet sich der Trager, und die LD gibt Licht aus.	-	Stromwert + 5,5mA auf dem Lasertonabnehmer markiert. Venn der Strom 40mA oder mehr über dem obigen Wert liegt, ist er defekt.	(b)
3	VCO	-	Einen Frequenzzähler an CN11(PLCK) anschließen. (X32-1170)	Die Spannungsversorgung aus- und dann wieder einschalten. Stop-Betriebsart	L3 (X32-1170)	4,27MHz	(c)
4	OPTISCHES GITTER	Testdisc Typ 4	Ein Oszilloskop wie folgt anschließen: Kanal 1: RF (X29-1870 Teststift) Kanal 2: TE (X32-1170 Stift 1)	Den Teststift kurzschließen und dabei die Spannungsversorgung einschalten, um den Testmodus zu aktivieren. Die CHECK-Taste drücken und prüfen, daß "0300" auf dem Display angezeigt wird.	-	Prüfen, ob das Beugungsgitter richtig ausgerichtet ist. (Das Gitter kann nicht eingestellt werden.)	(d)
5	SPURHALTEFEHLER-AUSGLEICH	Testdisc Typ 4	Ein Oszilloskop wie folgt anschließen: Kanal 1: RF (X29-1870 Teststift) Kanal 2: TE (X32-1170 Stift 1)	Den Teststift kurzschließen und dabei die Spannungsversorgung einschalten, um den Testmodus zu aktivieren. Die CHECK-Taste drücken und prüfen, daß "0300" auf dem Display angezeigt wird.	TE BALANCE YR3 (X29-1870)	Symetrie zwischen oberem und unterem Mustern oder Gleichstrom DC = 020,05V	(e)
6	FOKUS-FEHLERAUSGLEICH	Testdisc Typ 4	Ein Oszilloskop wie folgt anschließen: Kanal 1: RF (X29-1870 Teststift) Kanal 2: TE (X32-1170 Stift 1)	Die PLAY-Taste drücken und prüfen, daß "0500" auf dem Display angezeigt wird.	FOKUS-FEHLERAUSGLEICH YR4 (X29-1870)	Optimales Augenmuster	(f)
7	FOKUSVERSTÄRKUNG	Testdisc Type 4 Ein 900Hz, 40mV _{rms} Signal an Stift 2 von CN3 an platine X32-1170 anlegen.	Eine Servo-Lehre verwenden oder ein 47kΩ, 470pF Tiefpaßfilter an Stift 1 von CN3 anschließen.	Die Spannungsversorgung aus- und dann wieder einschalten, dann die PLAY-Taste drücken.	FOKUSVERSTÄRKUNG YR1 (X29-1870)	40mV _{rms}	(g)
8	SPURHALTE-VERSTÄRKUNG	Testdisc Type 4 Ein 900Hz, 40mV _{rms} Signal an Stift 4 von CN3 an platine X32-1170 anlegen.	Eine Servo-Lehre verwenden oder ein 47kΩ, 470pF Tiefpaßfilter an Stift 5 von CN3 anschließen.	PLAY	SPURHALTE-VERSTÄRKUNG YR2 (X29-1870)	40mV _{rms}	(g)
9	DAC-AUSGANG	Testdisc Typ 4	Ein Wechselstrom-Voltmeter an die Ausgangsklemme(FIXED) anschließen.	Das 1kHz, 0dB Signal in Titel Nr. 2 wiedergeben.	YR1: L YR2: R (X29-1870)	1,9~2,0V _{rms}	(b)
10	DAC-VERZERRUNG	Testdisc Typ 4	Ein Wechselstrom-Voltmeter an die Ausgangsklemme(FIXED) anschließen.	Das 1kHz, -20dB Signal in Titel Nr. 15 wiedergeben.	YR3: L YR4: R (X29-1870)	Minimale Verzerrung	(b)
11	DAC-VERZERRUNG	Testdisc Typ 4	Ein Wechselstrom-Voltmeter an die Ausgangsklemme(FIXED) anschließen.	Das 100Hz, 0dB Signal in Titel Nr. 4 wiedergeben.	YR5: L YR6: R (X29-1870)	Minimale Verzerrung	(h)

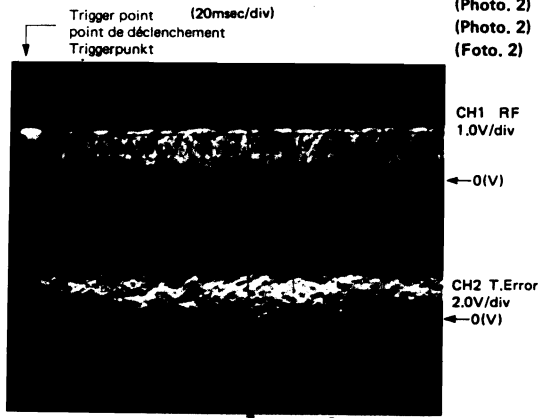
4. Description of Signal Waveforms, Connection of Measuring Instruments/Description des formes d'onde des signaux, connexion des instruments de mesure/Beschreibung der Signal-Wellenformen, Anschluß der Meßinstrumente



- RF signal and T.Error signal after diffraction grating adjustment.
- Signal RF et signal T.Error après ajustement de réseau de diffraction.
- RF-Signal und T.Error-Signal nach Diffraktionsgitter-Einstellung.

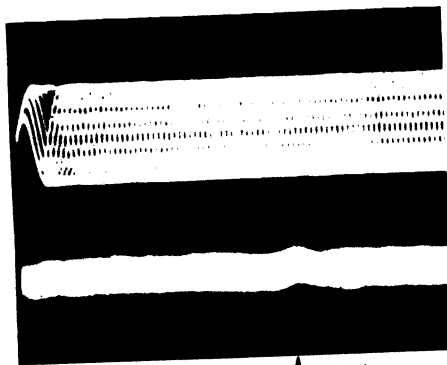


- RF signal and T.Error signal when there is small diffraction grating position error.
- The T.Error signal level is small, and the envelope is as shown in the diagram below.
- Signal RF et signal T.Error quand il y a une petite erreur de position du réseau de diffraction.
- Le niveau de signal T.Error est petit et l'enveloppe est telle qu'indiquée dans le diagramme ci-dessous.
- RF-Signal und T.Error-Signal bei kleinem Diffraktionsgitter-Positionierungsfehler.
- Der T.Error-Signalpegel ist klein, und die Hüllkurve ist wie in der Abbildung unten.



- RF signal and T.Error signal in test mode (with focusing ON).
- When the sub-beam traces the same bit series as the main beam during diffraction grating adjustment, bringing the RF trigger point to the position shown in the Photo causes a "projection" to be observed in the T.Error waveform.
- Le signal RF et le signal T.Error en mode de test (avec la mise au point sur ON).
- Quand un faisceau auxiliaire trace la même série de bits que le faisceau principal pendant l'ajustement de réseau de diffraction, l'apport du point de déclenchement RF à la position indiquée dans la photo provoque une "projection" qui s'observe dans la forme d'onde de T.Error.
- RF-Signal und T.Error-Signal im Testmodus (bei eingeschalteter Fokussierung).
- Wenn der Nebenstrahl die gleiche Bitreihe wie der Hauptstrahl während der Diffraktionsgitter-Einstellung verfolgt und den RF-Triggerpunkt auf die im Foto gezeigte Position bringt, wird eine "Hervorstehung" verursacht, die in der T.Error-Wellenform beobachtet werden kann.

ADJUSTMENT/REGLAGE/ABGLEICH

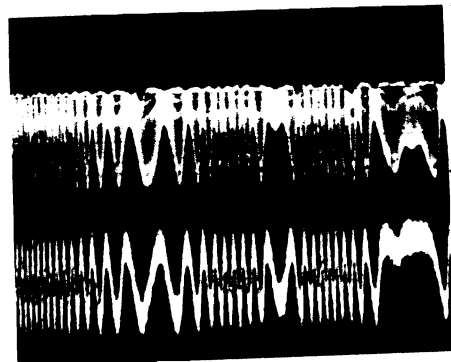


(2µsec/div) Projection
Projection
Hervorstehung

CH1 RF
1.0V/div
CH2 E.Spot
0.1V/div
AC coupling for
CH2 only
Couplage CA pour canal 2 seulement
AC-Kopplung nur für Kanal 2

(Photo. 4)
(Photo. 4)
(Foto. 4)

- RF signal and E.Spot signal in test mode (PLAY).
- If the diffraction grating has been adjusted properly, the influence of triggering is observed on the E.Spot waveform of approx. 12µs after RF signal, in the form of a projection.
- Signal RF et signal E.Spot en mode de test (PLAY).
- Si le réseau de diffraction a été ajusté correctement, l'influence du déclenchement s'observe sur la forme d'onde E.Spot d'environ 12µs après le signal RF, sous la forme d'une projection.
- RF-Signal und E.Spot-Signal im Testmodus (PLAY).
- Wenn das Diffraktionsgitter richtig eingestellt wurde, wird der Einfluß des Triggers in der E.Spot-Wellenform etwa 12µs nach dem RF-Signal in der Form einer Hervorstehung beobachtet.

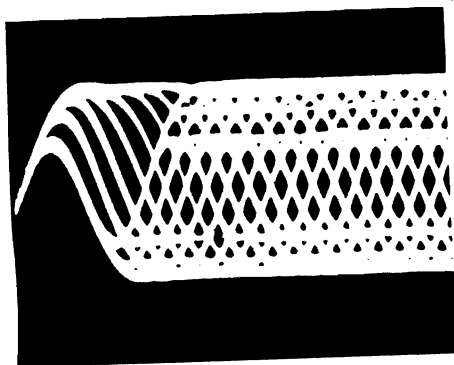


(20msec/div)

CH1 RF
1.0V/div
CH2 T.Error
2.0V/div

(Photo. 5)
(Photo. 5)
(Foto. 5)

- RF signal and T.Error signal: in test mode (Focusing ON) (Disc type 4)
- Adjust T.Error so that the waveform is symmetrical above and below 0V. (VR3 of X29-1780-00)
- Signal RF et signal T.Error: en mode test (mise au point ON). (Disque de type 4)
- Ajuster T.Error pour que la forme d'onde soit symétrique en-dessus et au-dessous de 0V. (VR3 de X29-1780-00)
- RF-Signal und T.Error-Signal: im Testmodus (Fokussierung eingeschaltet). (Disc-Typ 4)
- T.Error so einstellen, daß die Wellenform über und unter 0V symmetrisch ist. (VR3 von X29-1780-00)

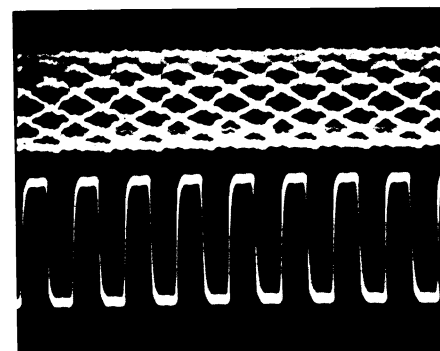


(0.5µsec/div)

(Photo. 6)
(Photo. 6)
(Foto. 6)

- RF signal in test mode (PLAY).
- Perform the tangential and focusing offset adjustments so that each of the center cross points are focused into one point on the display. The crossing points above and below the center shall also be displayed clearly.
- Signal RF en mode de test (PLAY).
- Effectuer les ajustements d'offset tangentiel et de mise au point pour que chacun des points de croisement central soit mis au point sur un point de l'affichage. Les points de croisement au-dessus et en-dessous du centre doivent aussi être affichés clairement.
- RF-Signal im Testmodus (PLAY).
- Die Tangential- und Fokusversatz-Einstellungen so durchführen, daß jeder der mittleren Kreuzungspunkte in einem Punkt auf dem Display fokussiert wird. Auch die Kreuzungspunkte über und unter der Mitte müssen klar angezeigt werden.

ADJUSTMENT/REGLAGE/ABGLEICH



(0.2µsec/div)

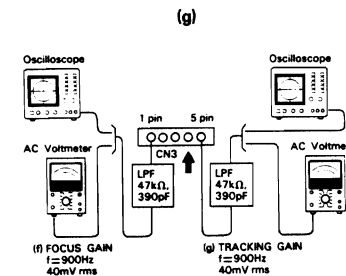
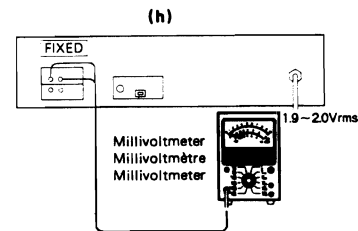
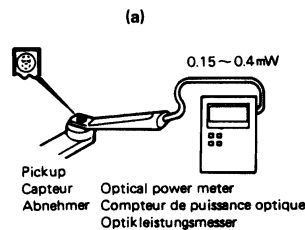
Eye pattern center
Centre de la forme oculaire
Augenmuster-Mitte

RF signal
1.0V/div

PLCK
2.0V/div

(Photo. 7)
(Photo. 7)
(Foto. 7)

- RF signal and PLCK signal in test mode (PLAY).
- When the synch system is normal, the cross points at the center of the eye pattern shall coincide with the PLCK fall points.
- Le signal RF et le signal PLCK en mode de test (PLAY).
- Quand le système sync est normal, les points de croisement au centre de la forme oculaire doivent coïncider avec les points de chute PLCK.
- RF-Signal und PLCK-Signal im Testmodus (PLAY).
- Wenn das Sync-System normal ist, müssen die Kreuzungspunkte in der Mitte des Augenmusters mit den PLCK-Fallpunkten zusammenfallen.



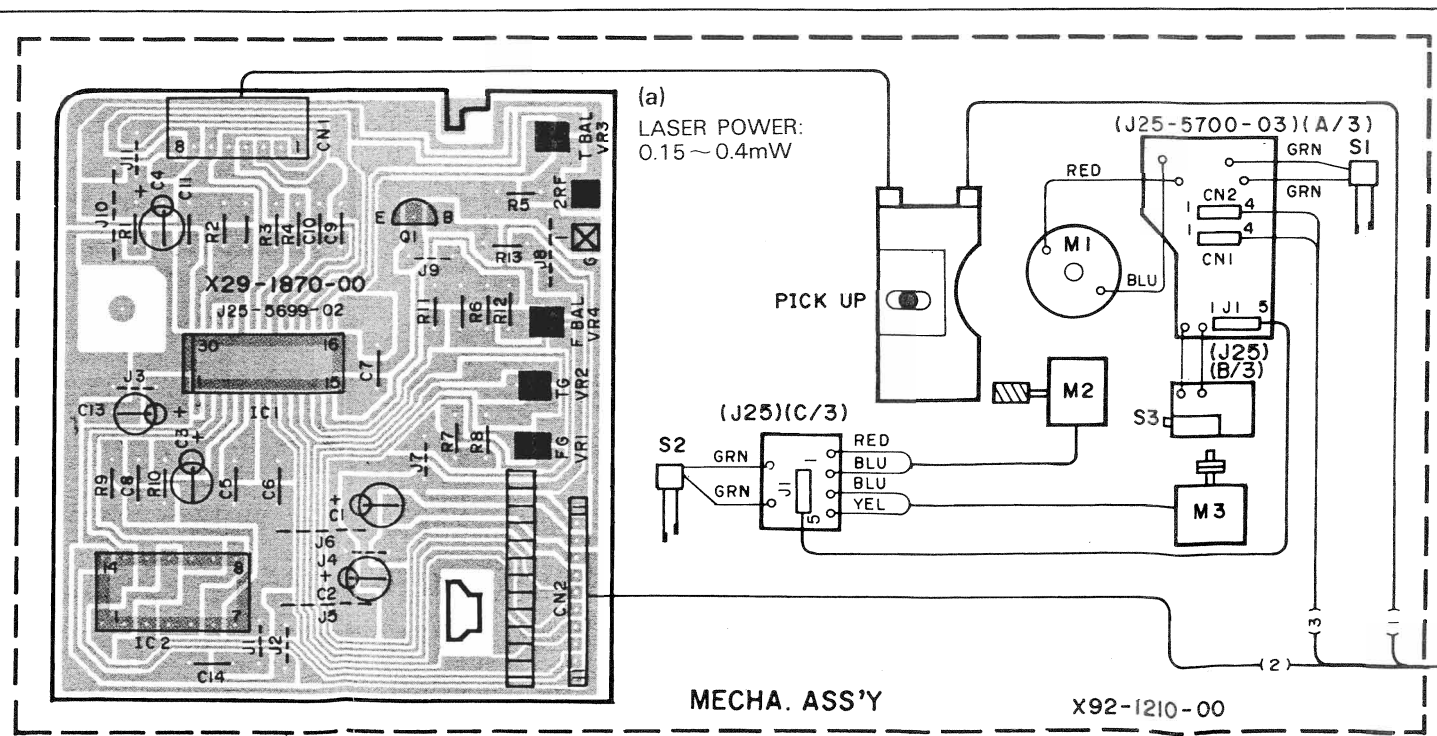
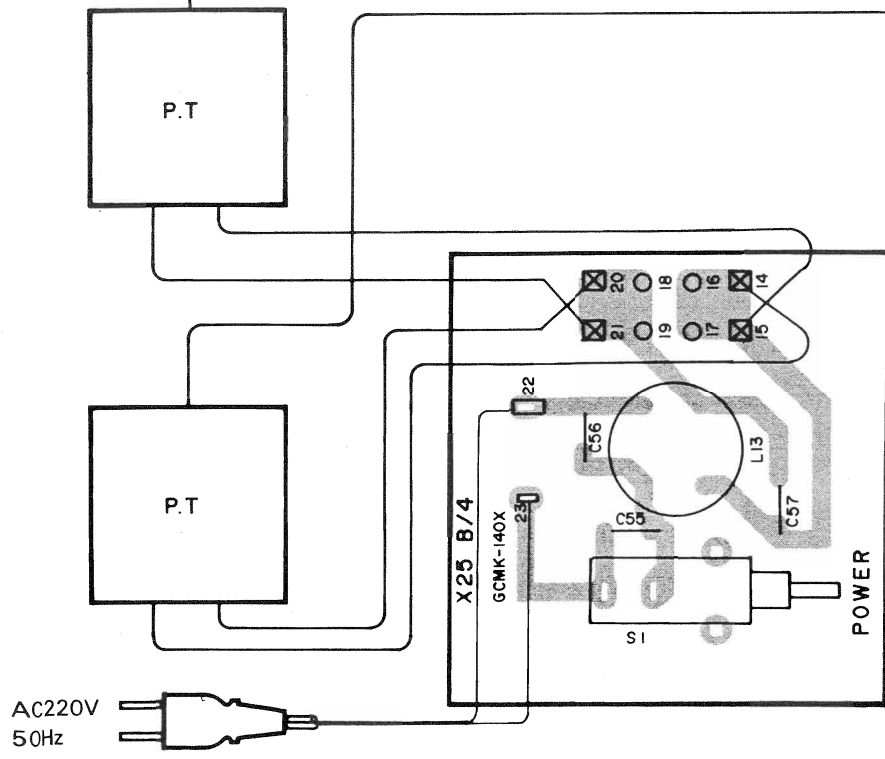
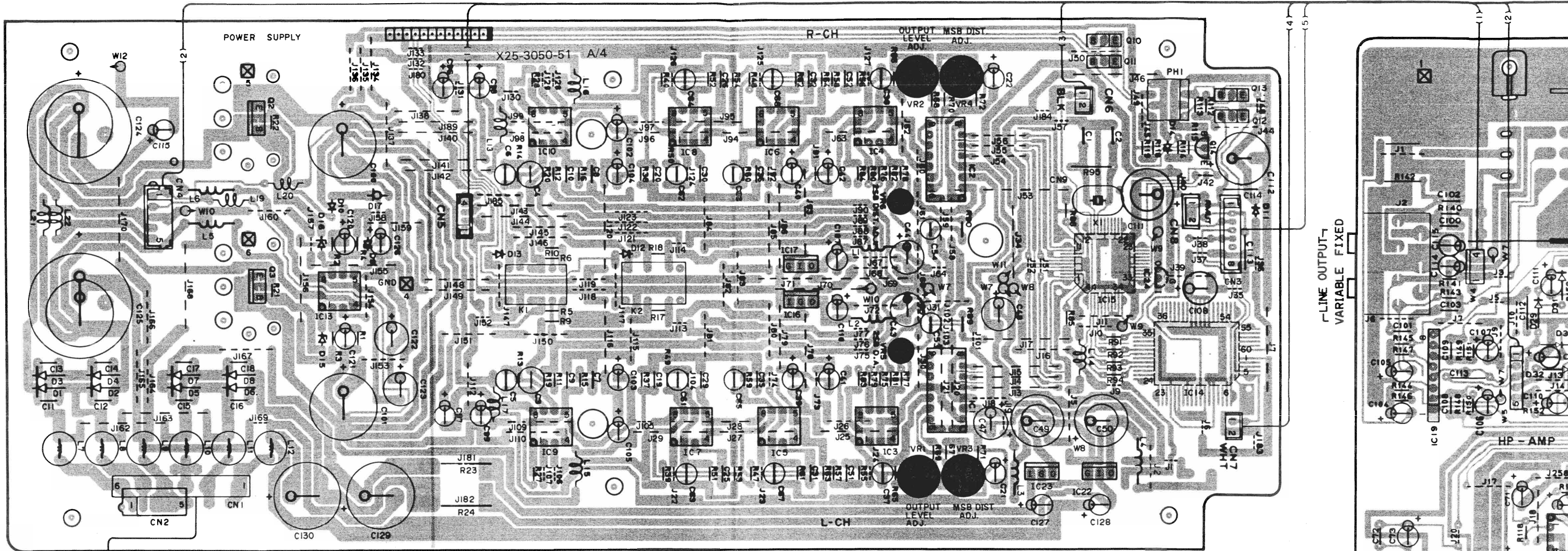
(f) FOCUS GAIN
f=300Hz
40mV rms

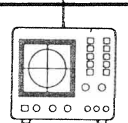
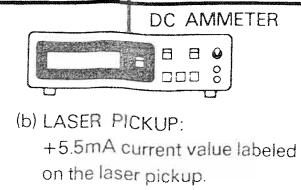
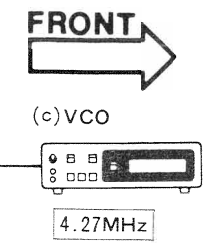
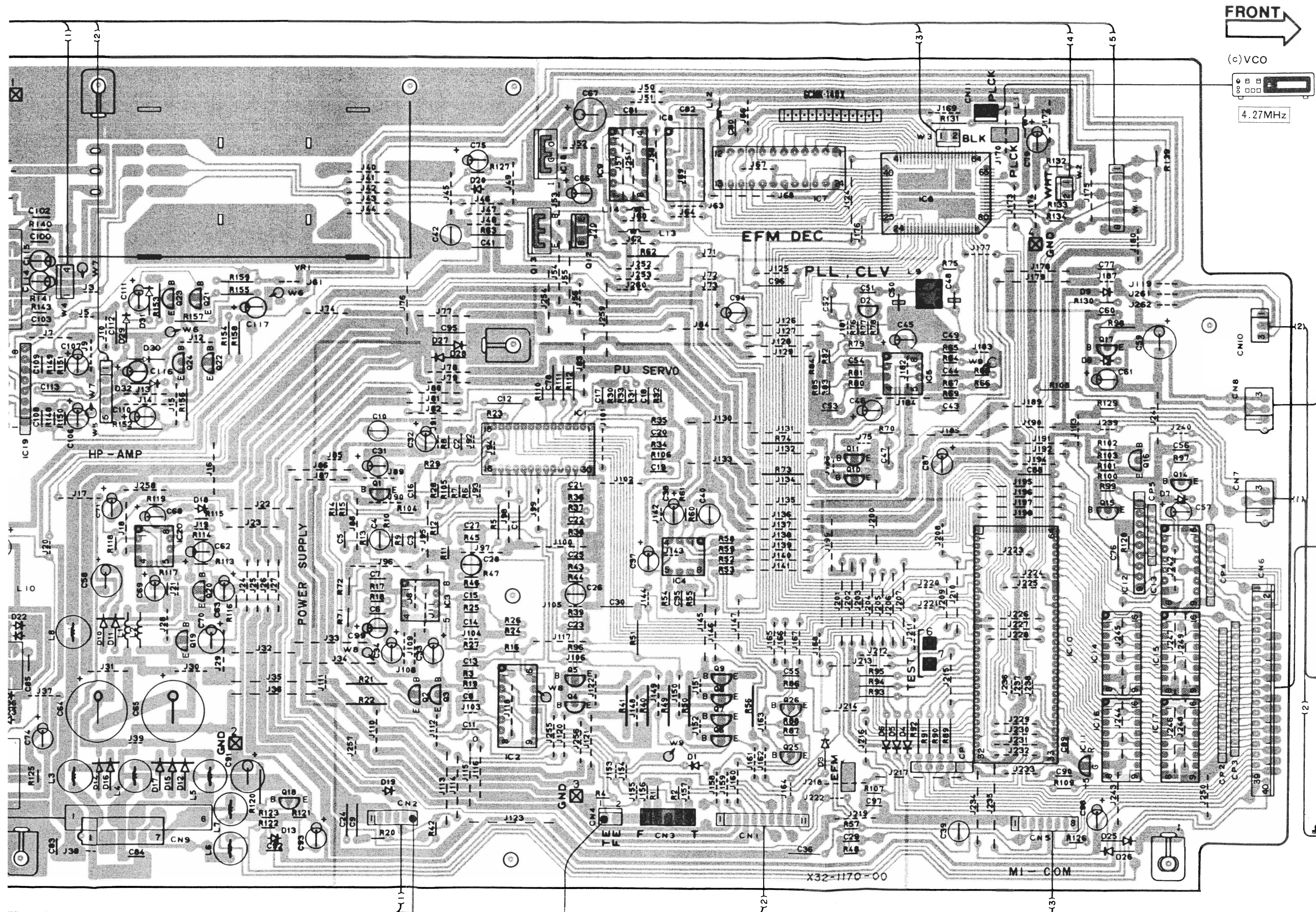
(g) TRACKING GAIN
f=300Hz
40mV rms

VOLTAGE CHECK TABLE

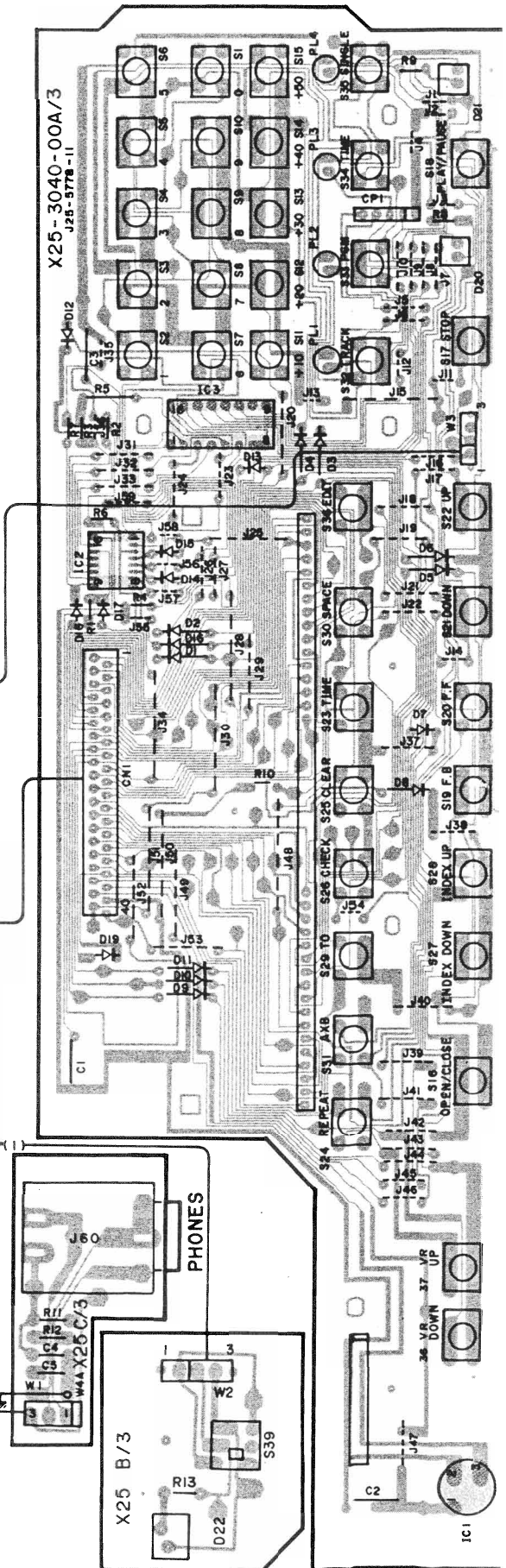
(X25-3040-00)				(X25-3050-00)				(X32-1170-00)				(X-92-1210-00)																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																								
IC1	1 0V	2 4.9V	3 4.9V	IC1	1 -5.6V	2 0V	3 4.9V	IC8	1 0V	2 0.1V	3 0V	IC14	1 0V	2 4.7V	3 0V	IC15	1 -0.1V	2 0V	3 0V	IC1	1 0V	2 0V	3 0V	IC6	1 0V	2 0V	3 0V	IC7	1 2.3V	2 2.3V	3 3.5V	IC10	1 2.9V	2 3.5V	3 5.1V	IC12	1 5.6V	2 5.1V	3 5.1V	IC16	1 0.3V	2 0.3V	3 0.3V	IC1	1 0V	2 0V	3 0V																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																					
IC2	4 -4.8V	5 1.3V	6 2.4V	IC3	4 -4.8V	5 1.3V	6 2.4V	IC9	4 -15.6V	5 0V	6 -0.1V	IC11	4 2.2V	5 0V	6 2.4V	IC12	4 0V	5 0V	6 0V	IC13	4 0V	5 0V	6 0V	IC17	4 0V	5 0V	6 0V	IC18	4 0V	5 0V	6 0V	IC19	4 0V	5 0V	6 0V	IC20	4 0V	5 0V	6 0V	IC21	4 0V	5 0V	6 0V	IC22	4 0V	5 0V	6 0V	IC23	4 0V	5 0V	6 0V	IC24	4 0V	5 0V	6 0V	IC25	4 0V	5 0V	6 0V	IC26	4 0V	5 0V	6 0V	IC27	4 0V	5 0V	6 0V	IC28	4 0V	5 0V	6 0V	IC29	4 0V	5 0V	6 0V	IC30	4 0V	5 0V	6 0V	IC31	4 0V	5 0V	6 0V	IC32	4 0V	5 0V	6 0V	IC33	4 0V	5 0V	6 0V	IC34	4 0V	5 0V	6 0V	IC35	4 0V	5 0V	6 0V	IC36	4 0V	5 0V	6 0V	IC37	4 0V	5 0V	6 0V	IC38	4 0V	5 0V	6 0V	IC39	4 0V	5 0V	6 0V	IC40	4 0V	5 0V	6 0V	IC41	4 0V	5 0V	6 0V	IC42	4 0V	5 0V	6 0V	IC43	4 0V	5 0V	6 0V	IC44	4 0V	5 0V	6 0V	IC45	4 0V	5 0V	6 0V	IC46	4 0V	5 0V	6 0V	IC47	4 0V	5 0V	6 0V	IC48	4 0V	5 0V	6 0V	IC49	4 0V	5 0V	6 0V	IC50	4 0V	5 0V	6 0V	IC51	4 0V	5 0V	6 0V	IC52	4 0V	5 0V	6 0V	IC53	4 0V	5 0V	6 0V	IC54	4 0V	5 0V	6 0V	IC55	4 0V	5 0V	6 0V	IC56	4 0V	5 0V	6 0V	IC57	4 0V	5 0V	6 0V	IC58	4 0V	5 0V	6 0V	IC59	4 0V	5 0V	6 0V	IC60	4 0V	5 0V	6 0V	IC61	4 0V	5 0V	6 0V	IC62	4 0V	5 0V	6 0V	IC63	4 0V	5 0V	6 0V	IC64	4 0V	5 0V	6 0V	IC65	4 0V	5 0V	6 0V	IC66	4 0V	5 0V	6 0V	IC67	4 0V	5 0V	6 0V	IC68	4 0V	5 0V	6 0V	IC69	4 0V	5 0V	6 0V	IC70	4 0V	5 0V	6 0V	IC71	4 0V	5 0V	6 0V	IC72	4 0V	5 0V	6 0V	IC73	4 0V	5 0V	6 0V	IC74	4 0V	5 0V	6 0V	IC75	4 0V	5 0V	6 0V	IC76	4 0V	5 0V	6 0V	IC77	4 0V	5 0V	6 0V	IC78	4 0V	5 0V	6 0V	IC79	4 0V	5 0V	6 0V	IC80	4 0V	5 0V	6 0V	IC81	4 0V	5 0V	6 0V	IC82	4 0V	5 0V	6 0V	IC83	4 0V	5 0V	6 0V	IC84	4 0V	5 0V	6 0V	IC85	4 0V	5 0V	6 0V	IC86	4 0V	5 0V	6 0V	IC87	4 0V	5 0V	6 0V	IC88	4 0V	5 0V	6 0V	IC89	4 0V	5 0V	6 0V	IC90	4 0V	5 0V	6 0V	IC91	4 0V	5 0V	6 0V	IC92	4 0V	5 0V	6 0V	IC93	4 0V	5 0V	6 0V	IC94	4 0V	5 0V	6 0V	IC95	4 0V	5 0V	6 0V	IC96	4 0V	5 0V	6 0V	IC97	4 0V	5 0V	6 0V	IC98	4 0V	5 0V	6 0V	IC99	4 0V	5 0V	6 0V	IC100	4 0V	5 0V	6 0V	IC101	4 0V	5 0V	6 0V	IC102	4 0V	5 0V	6 0V	IC103	4 0V	5 0V	6 0V	IC104	4 0V	5 0V	6 0V	IC105	4 0V	5 0V	6 0V	IC106	4 0V	5 0V	6 0V	IC107	4 0V	5 0V	6 0V	IC108	4 0V	5 0V	6 0V	IC109	4 0V	5 0V	6 0V	IC110	4 0V	5 0V	6 0V	IC111	4 0V	5 0V	6 0V	IC112	4 0V	5 0V	6 0V	IC113	4 0V	5 0V	6 0V	IC114	4 0V	5 0V	6 0V	IC115	4 0V	5 0V	6 0V	IC116	4 0V	5 0V	6 0V	IC117	4 0V	5 0V	6 0V	IC118	4 0V	5 0V	6 0V	IC119	4 0V	5 0V	6 0V	IC120	4 0V	5 0V	6 0V	IC121	4 0V	5 0V	6 0V	IC122	4 0V	5 0V	6 0V	IC123	4 0V	5 0V	6 0V	IC124	4 0V	5 0V	6 0V	IC125	4 0V	5 0V	6 0V	IC126	4 0V	5 0V	6 0V	IC127	4 0V	5 0V	6 0V	IC128	4 0V	5 0V	6 0V	IC129	4 0V	5 0V	6 0V	IC130	4 0V	5 0V	6 0V	IC131	4 0V	5 0V	6 0V	IC132	4 0V	5 0V	6 0V	IC133	4 0V	5 0V	6 0V	IC134	4 0V	5 0V	6 0V	IC135	4 0V	5 0V	6 0V	IC136	4 0V	5 0V	6 0V	IC137	4 0V	5 0V	6 0V	IC138	4 0V	5 0V	6 0V	IC139	4 0V	5 0V	6 0V	IC140	4 0V	5 0V	6 0V	IC141	4 0V	5 0V	6 0V	IC142	4 0V	5 0V	6 0V	IC143	4 0V	5 0V	6 0V	IC144	4 0V	5 0V	6 0V	IC145	4 0V	5 0V	6 0V	IC146	4 0V	5 0V	6 0V	IC147	4 0V	5 0V	6 0V	IC148	4 0V	5 0V	6 0V	IC149	4 0V	5 0V	6 0V	IC150	4 0V	5 0V	6 0V	IC151	4 0V	5 0V	6 0V	IC152	4 0V	5 0V	6 0V	IC153	4 0V	5 0V	6 0V	IC154	4 0V	5 0V	6 0V	IC155	4 0V	5 0V	6 0V	IC156	4 0V	5 0V	6 0V	IC157	4 0V	5 0V	6 0V	IC158	4 0V	5 0V	6 0V	IC159	4 0V	5 0V	6 0V	IC160	4 0V	5 0V	6 0V	IC161	4 0V	5 0V	6 0V	IC162	4 0V	5 0V	6 0V	IC163	4 0V	5 0V	6 0V	IC164	4 0V	5 0V	6 0V	IC165	4 0V	5 0V	6 0V	IC166	4 0V	5 0V	6 0V	IC167	4 0V	5 0V	6 0V	IC168	4 0V	5 0V	6 0V	IC169	4 0V	5 0V	6 0V	IC170	4 0V	5 0V	6 0V	IC171	4 0V	5 0V	6 0V	IC172	4 0V	5 0V	6 0V	IC173	4 0V	5 0V	6 0V	IC174	4 0V	5 0V	6 0V	IC175	4 0V	5 0V	6 0V	IC176	4 0V	5 0V	6 0V	IC177	4 0V	5 0V	6 0V	IC178	4 0V	5 0V	6 0V	IC179	4 0V	5 0V	6 0V	IC180	4 0V	5 0V	6 0V	IC181	4 0V	5 0V	6 0V	IC182	4 0V	5 0V	6 0V	IC183	4 0V	5 0V	6 0V	IC184	4 0V	5 0V	6 0V	IC185	4 0V	5 0V	6 0V	IC186	4 0V	5 0V	6 0V	IC187	4 0V	5 0V	6 0V	IC188	4 0V	5 0V	6 0V	IC189	4 0V	5 0V	6 0V	IC190	4 0V	5 0V	6 0V	IC191	4 0V	5 0V	6 0V	IC192	4 0V	5 0V	6 0V	IC193	4 0V	5 0V	6 0V	IC194	4 0V	5 0V	6 0V	IC195	4 0V	5 0V	6 0V	IC196	4 0V	5 0V	6 0V	IC197	4 0V	5 0V	6 0V	IC198	4 0V	5 0V	6 0V	IC199	4 0V	5 0V	6 0V	IC200	4 0V	5 0V	6 0V	IC201	4 0V	5 0V	6 0V	IC202	4 0V	5 0V	6 0V	IC203	4 0V	5 0V	6 0V	IC204	4 0V	5 0V	6 0V	IC205	4 0V	5 0V	6 0V	IC206	4 0V	5 0V	6 0V	IC207	4 0V	5 0V	6 0V	IC208	4 0V	5 0V	6 0V	IC209	4 0V	5 0V	6 0V	IC210	4 0V	5 0V	6 0V	IC211	4 0V	5 0V	6 0V	IC212	4 0V	5 0V	6 0V	IC213	4 0V	5 0V	6 0V	IC214	4 0V	5 0V	6 0V	IC215	4 0V	5 0V	6 0V	IC216	4 0V	5 0V	6 0V	IC217	4 0V	5 0V	6 0V	IC218	4 0V	5 0V	6 0V	IC219	4 0V	5 0V	6 0V	IC220	4 0V	5 0V	6 0V	IC221	4 0V	5 0V	6 0V	IC222	4 0V	5 0V	6 0V	IC223	4 0V	5 0V	6 0V	IC224	4 0V	5 0V	6 0V	IC225	4 0V	5 0V	6 0V	IC226	4 0V	5 0V	6 0V	IC227	4 0V	5 0V	6 0V	IC228	4 0V	5 0V	6 0V	IC229	4 0V	5 0V	6 0V	IC230	4 0V	5 0V	6 0V	IC231	4 0V	5 0V	6 0V	IC232	4 0V	5 0V	6 0V	IC233	4 0V	5 0V	6 0V	IC234	4 0V	5 0V	6 0V	IC235	4 0V	5 0V	6 0V	IC236	4 0V	5 0V	6 0V	IC237	4 0V	5 0V	6 0V	IC238	4 0V	5 0V	6 0V	IC239	4 0V	5 0V	6 0V	IC240	4 0V	5 0V	6 0V	IC241	4 0V	5 0V	6 0V	IC242	4 0V	5 0V	6 0V	IC243	4 0V	5 0V	6 0V	IC244	4 0V	5 0V	6 0V	IC245	4 0V	5 0V	6 0V	IC246	4 0V	5 0V	6 0V	IC247	4 0V	5 0V	6 0V	IC248	4 0V	5 0V	6 0V	IC249	4 0V	5 0V	6 0V	IC250	4 0V	5 0V	6 0V	IC251	4 0V	5 0V	6 0V	IC252	4 0V	5 0V	6 0V	IC253	4 0V	5 0V	6 0V	IC254	4 0V	5 0V	6 0V	IC255	4 0V	5 0V	6 0V	IC256	4 0V	5 0V	6 0V	IC257	4 0V	5 0V	6 0V	IC258	4 0V	5 0V	6 0V	IC259	4 0V	5 0V	6 0V	IC260	4 0V	5 0V	6 0V	IC261	4 0V	5 0V	6 0V	IC262	4 0V	5 0V	6 0V	IC263	4 0V	5 0V	6 0V	IC264	4 0V	5 0V	6 0V	IC265	4 0V	5 0V	6 0V	IC266	4 0V	5 0V	6 0V	IC267	4 0V	5 0V	6 0V	IC268	4 0V	5 0V	6 0V	IC269	4 0V	5 0V	6 0V	IC270	4 0V	5 0V	6 0V	IC271	4 0V	5 0V	6 0V	IC272	4 0V	5 0V	6 0V	IC273	4 0V	5 0V	6 0V	IC274	4 0V	5 0V	6 0V	IC275	4 0V	5 0V	6 0V	IC276

PC BOARD (Component Side View)



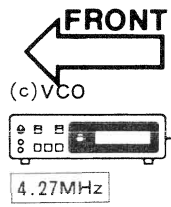
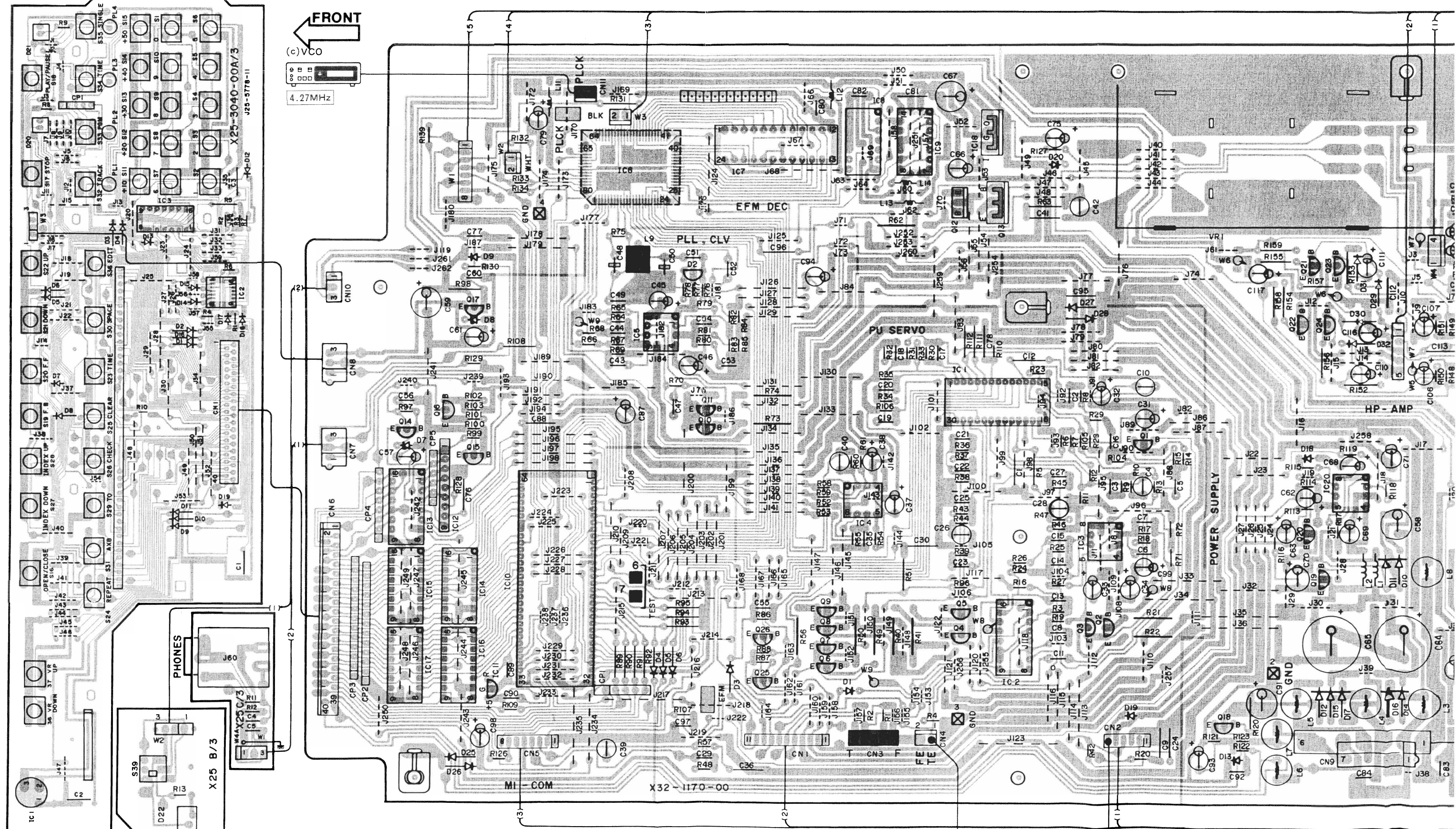


- (d) DIFFRACTION GRATING:
Check that the diffraction grating is aligned correctly.
- (e) TRACKING ERROR BALANCE:
Symmetry between upper and lower patterns, or
DC = 0 ± 0.05V
- (f) FOCUS ERROR BALANCE: Optimum eye pattern

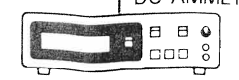
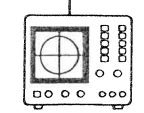


Refer to the schematic diagram for the values of resistors and capacitors.

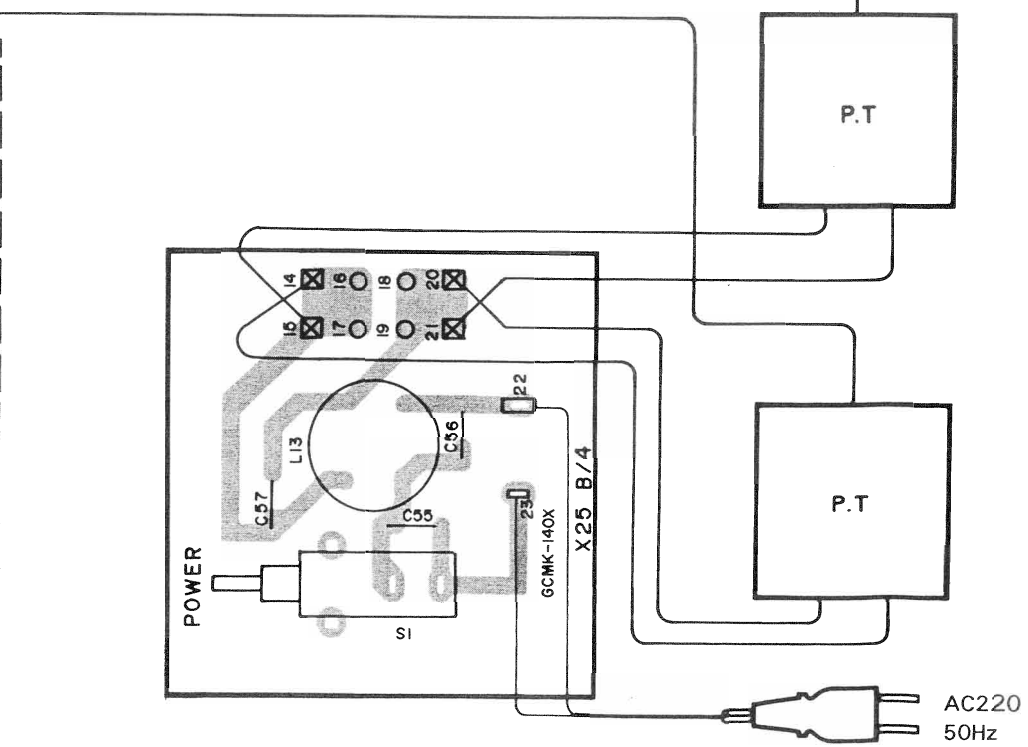
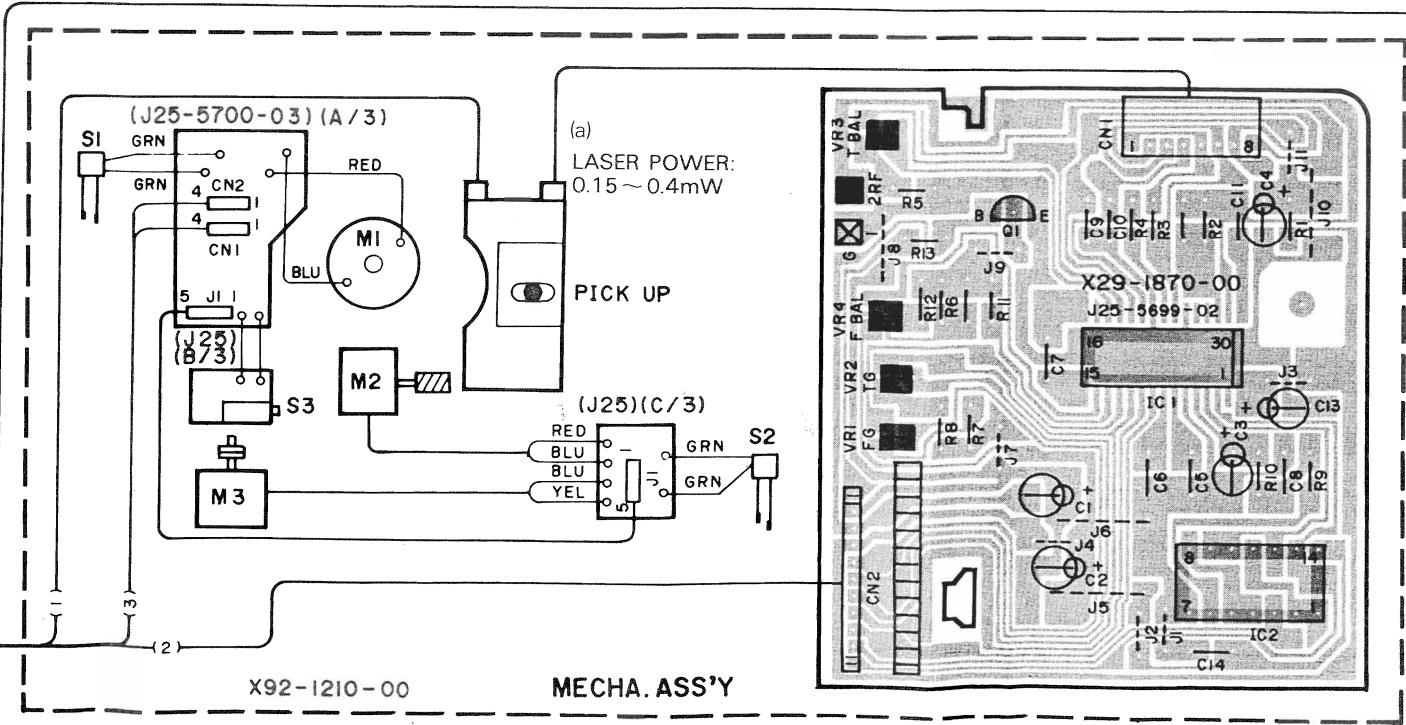
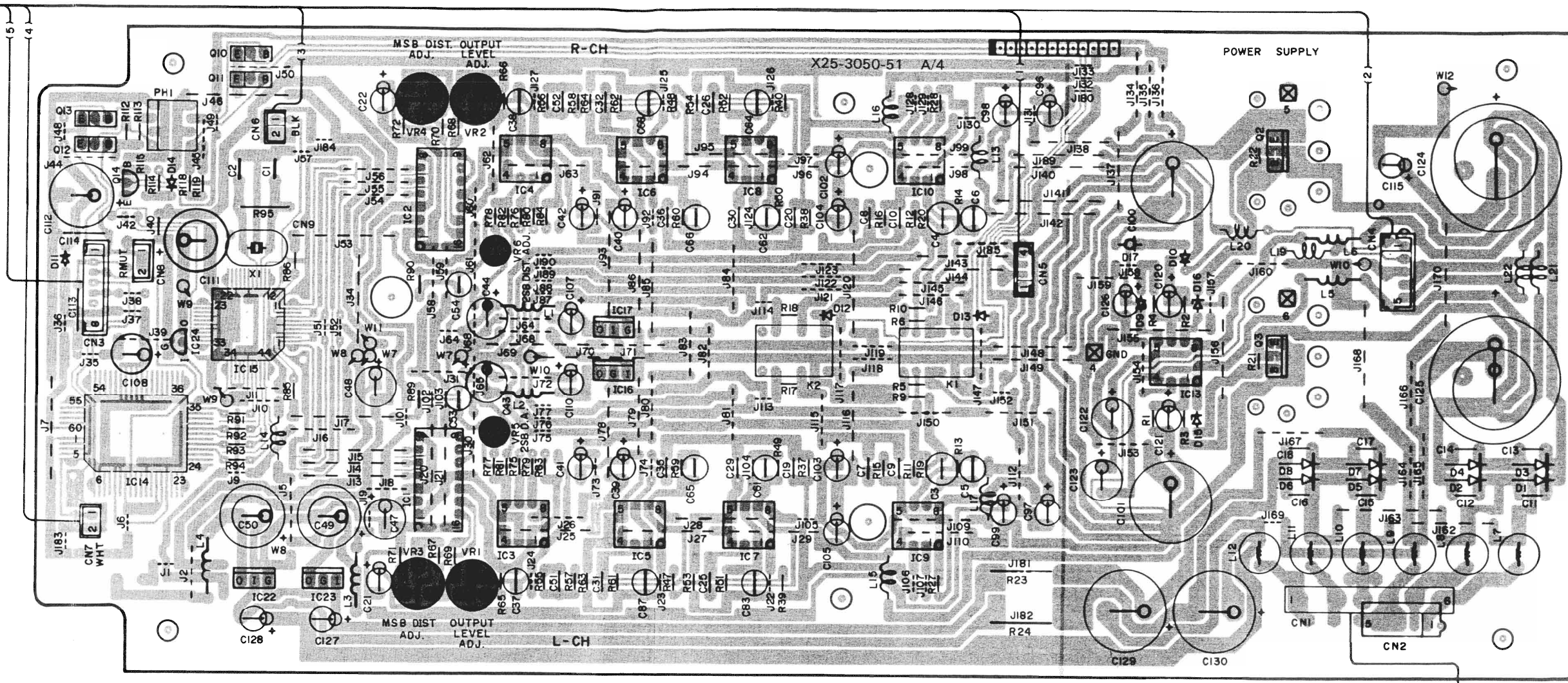
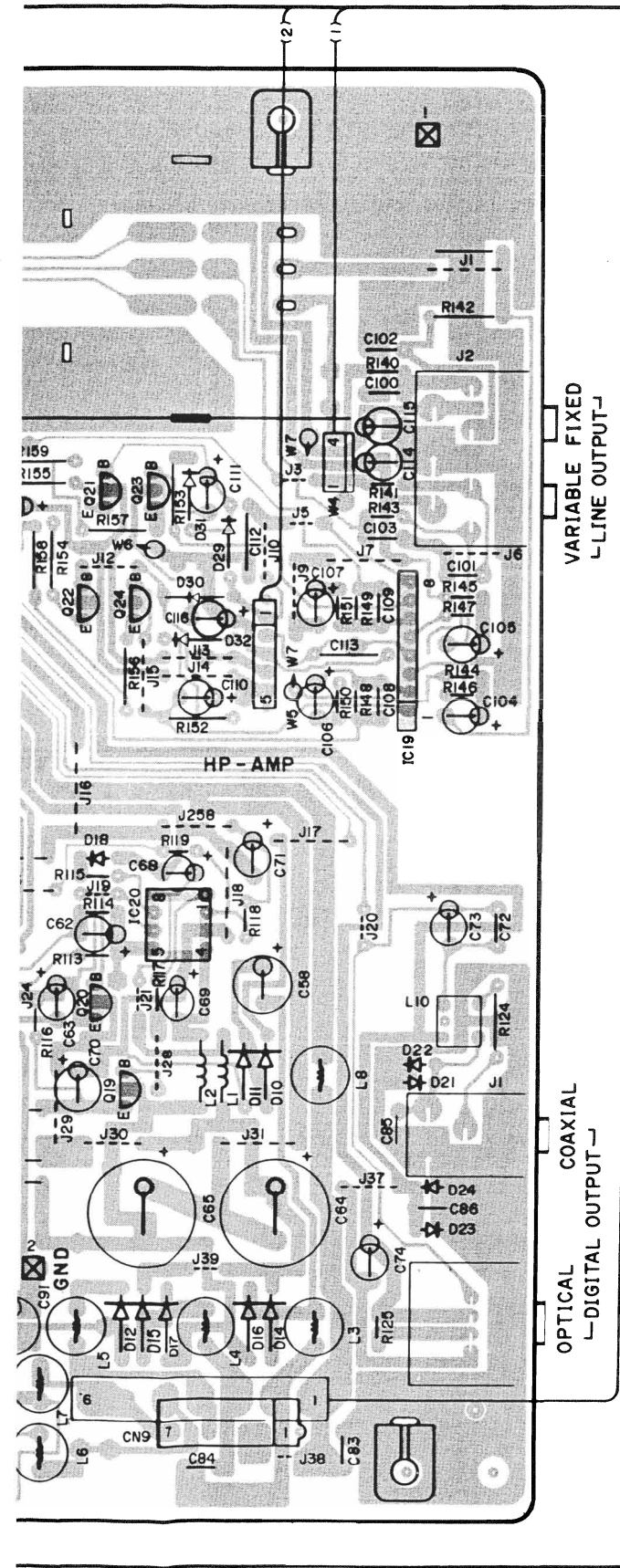
PC BOARD (Foil Side View)

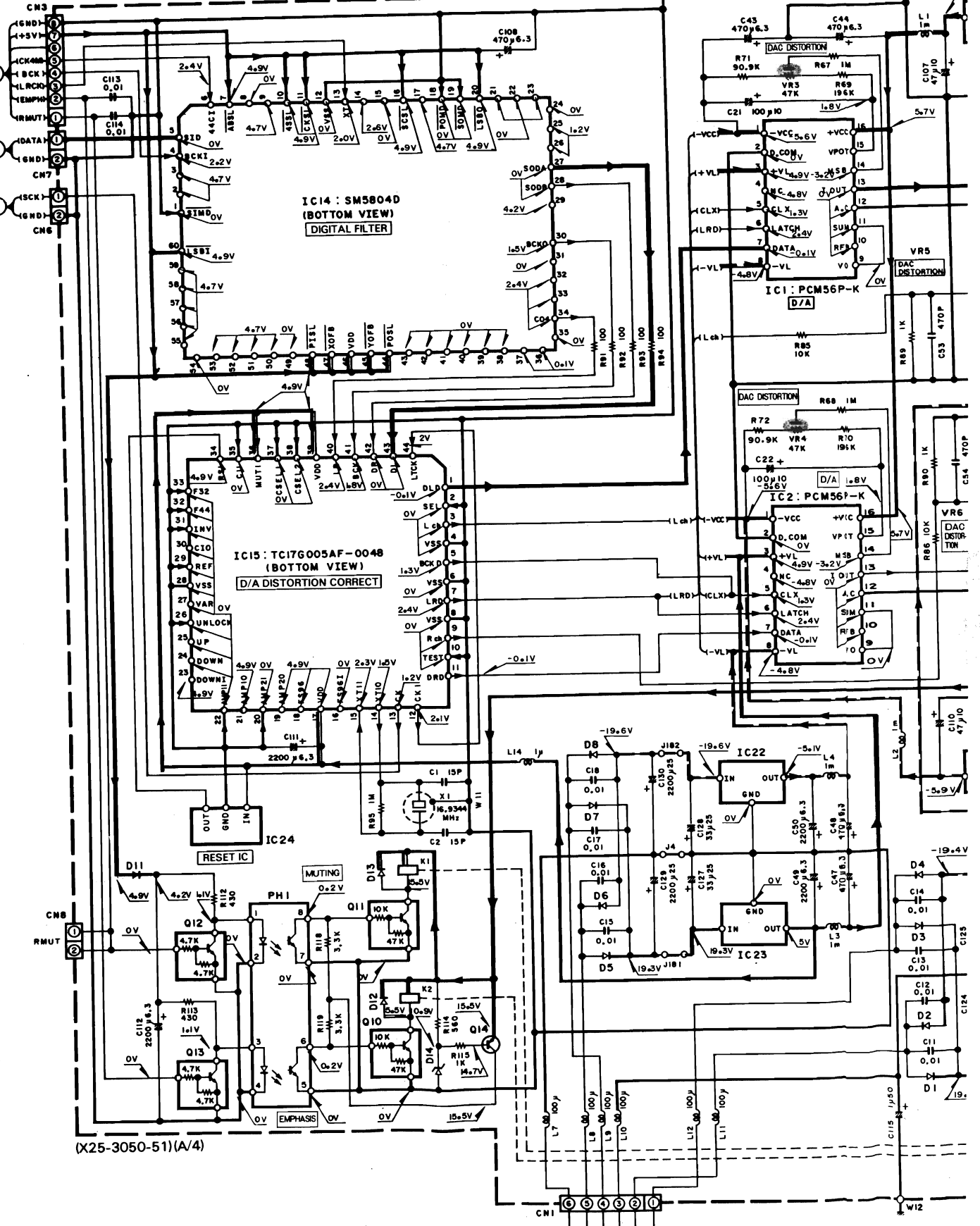
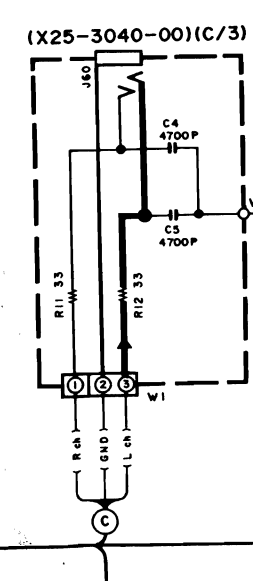
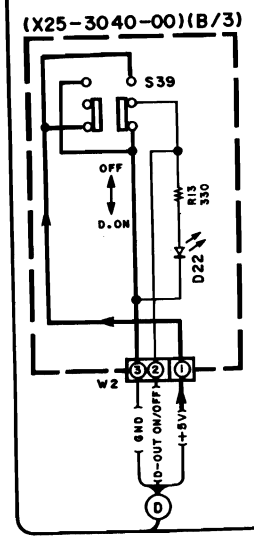
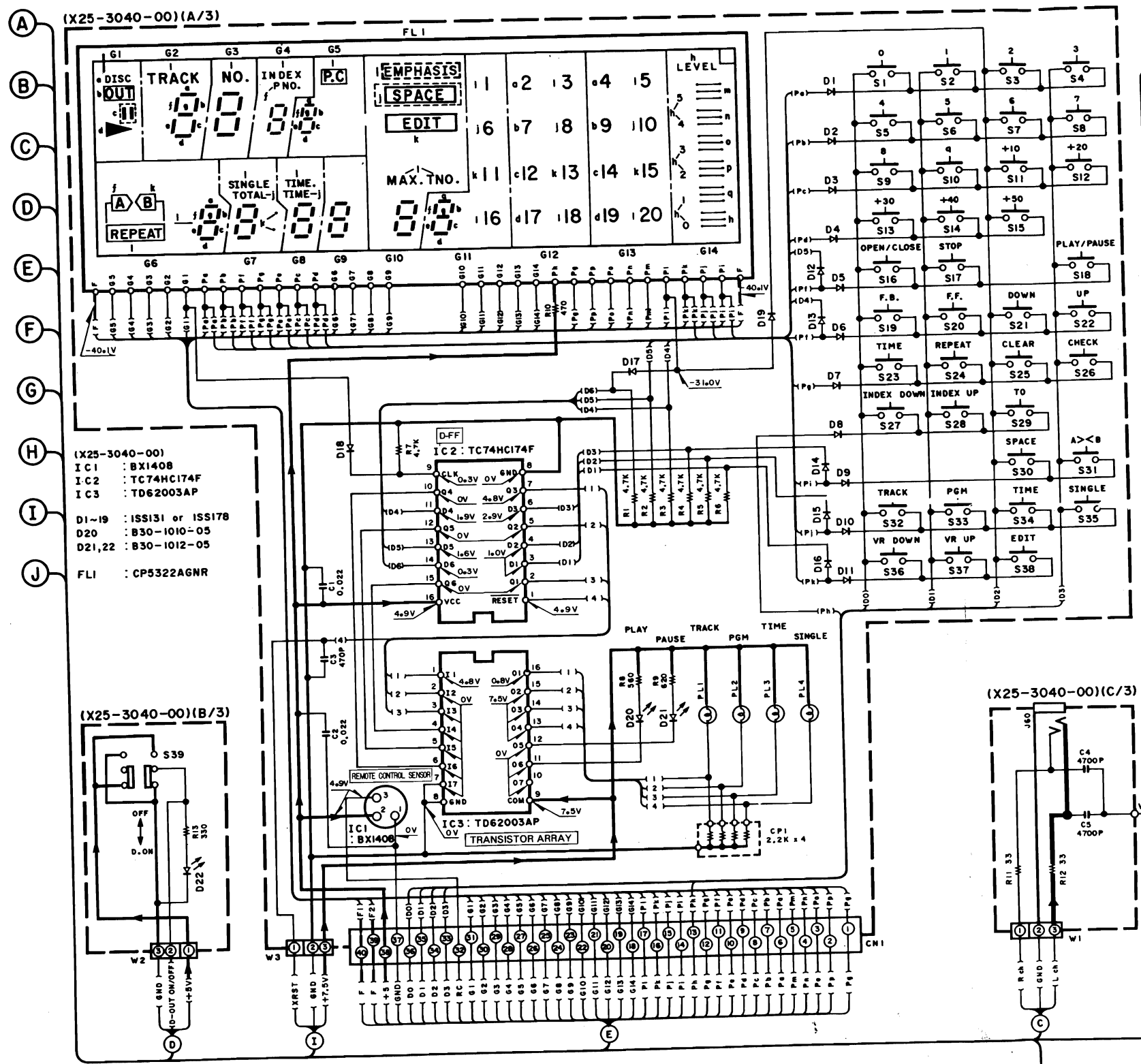


- (d) DIFFRACTION GRATING: Check that the diffraction grating is aligned correctly.
- (e) TRACKING ERROR BALANCE: Symmetry between upper and lower patterns, or $DC = 0 \pm 0.05V$
- (f) FOCUS ERROR BALANCE: Optimum eye pattern

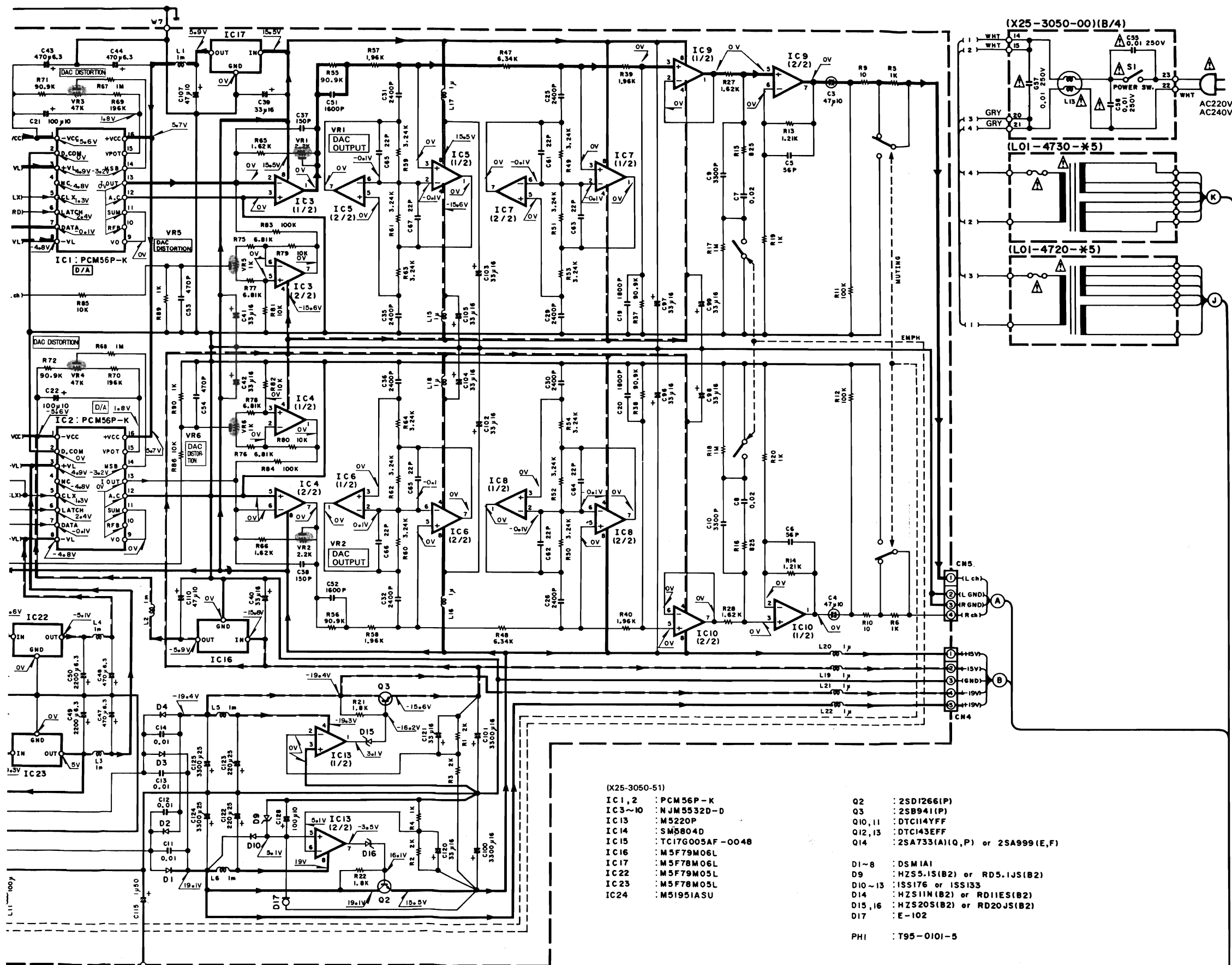


(b) LASER PICKUP: +5.5mA current value labeled on the laser pickup.





— SIGNAL LINE
 — GND LINE
 — +B LINE
 - - - -B LINE



- (X25-3050-51)
- | | | | |
|--------|-------------------|---------|---------------------------------|
| IC1, 2 | : PCM56P-K | Q2 | : 2SD1266(P) |
| IC3-10 | : NJM5532D-D | Q3 | : 2SB941(P) |
| IC13 | : M5220P | Q10, 11 | : DTC114YFF |
| IC14 | : SM5804D | Q12, 13 | : DTC143EFF |
| IC15 | : TC17G005AF-0048 | Q14 | : 2SA733(A)(Q,P) or 2SA999(E,F) |
| IC16 | : M5F79M06L | | |
| IC17 | : M5F78M06L | D1-8 | : DSM1A1 |
| IC22 | : M5F79M05L | D9 | : HZS5-1S(B2) or RD5-1JS(B2) |
| IC23 | : M5F78M05L | D10-13 | : ISS176 or ISS133 |
| IC24 | : M51951ASU | D14 | : HZS11M(B2) or RD11ES(B2) |
| | | D15, 16 | : HZS20S(B2) or RD20JS(B2) |
| | | D17 | : E-102 |
| | | PHI | : T95-0101-5 |

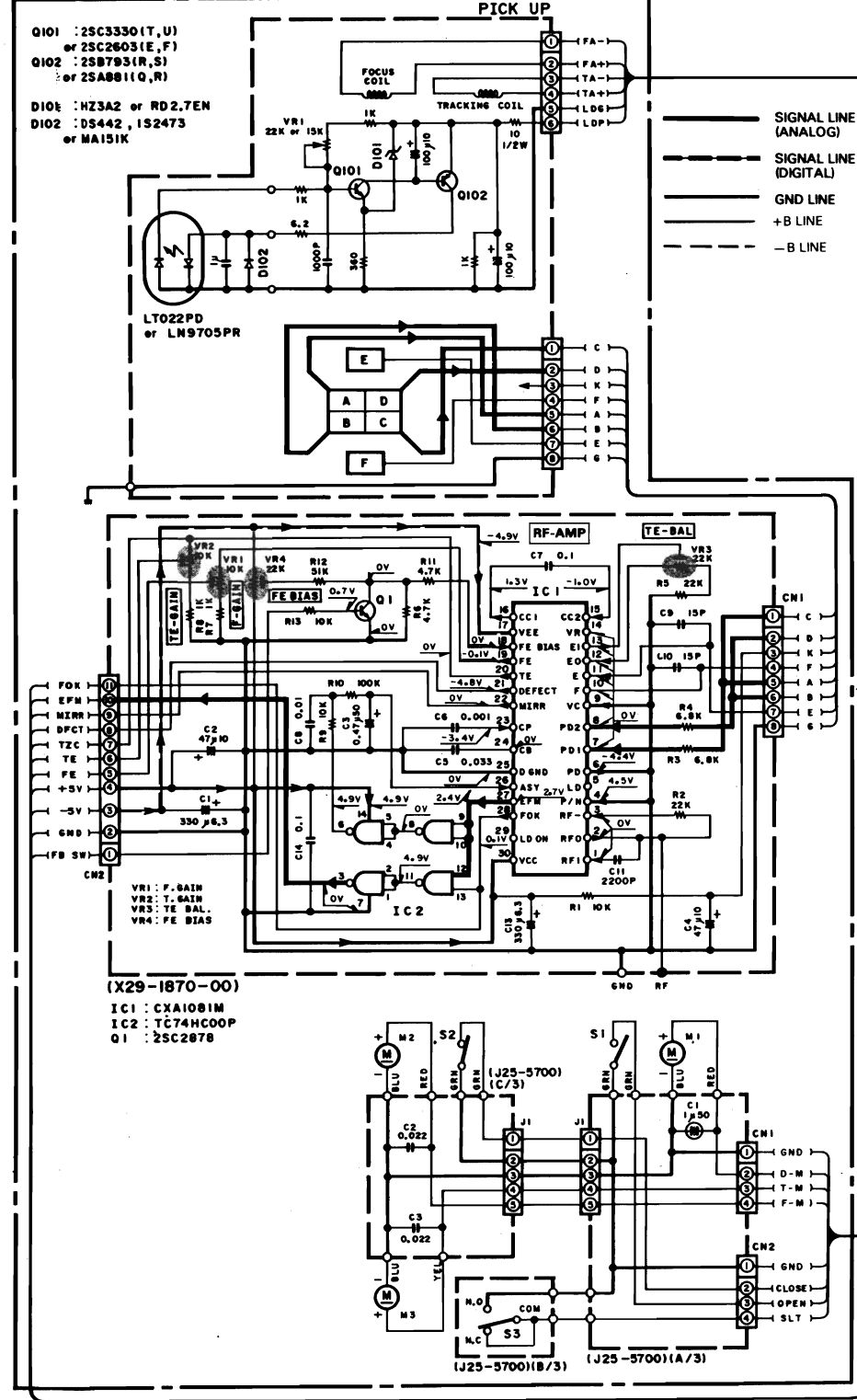
CAUTION: For continued safety, replace safety critical components only with manufacturer's recommended parts (refer to parts list). Indicates safety critical components. To reduce the risk of electric shock, leakage-current or resistance measurements shall be carried out (exposed parts are acceptably insulated from the supply circuit) before the appliance is returned to the customer.

• DC voltages are measured with a high impedance voltmeter. Values may vary slightly due to variations between individual instruments or/and units.
 • Les tensions c.c. doivent être mesurées avec un voltmètre à haute impédance. Les valeurs peuvent différer légèrement du fait des variations inhérentes aux appareils et aux instruments de mesure individuels.

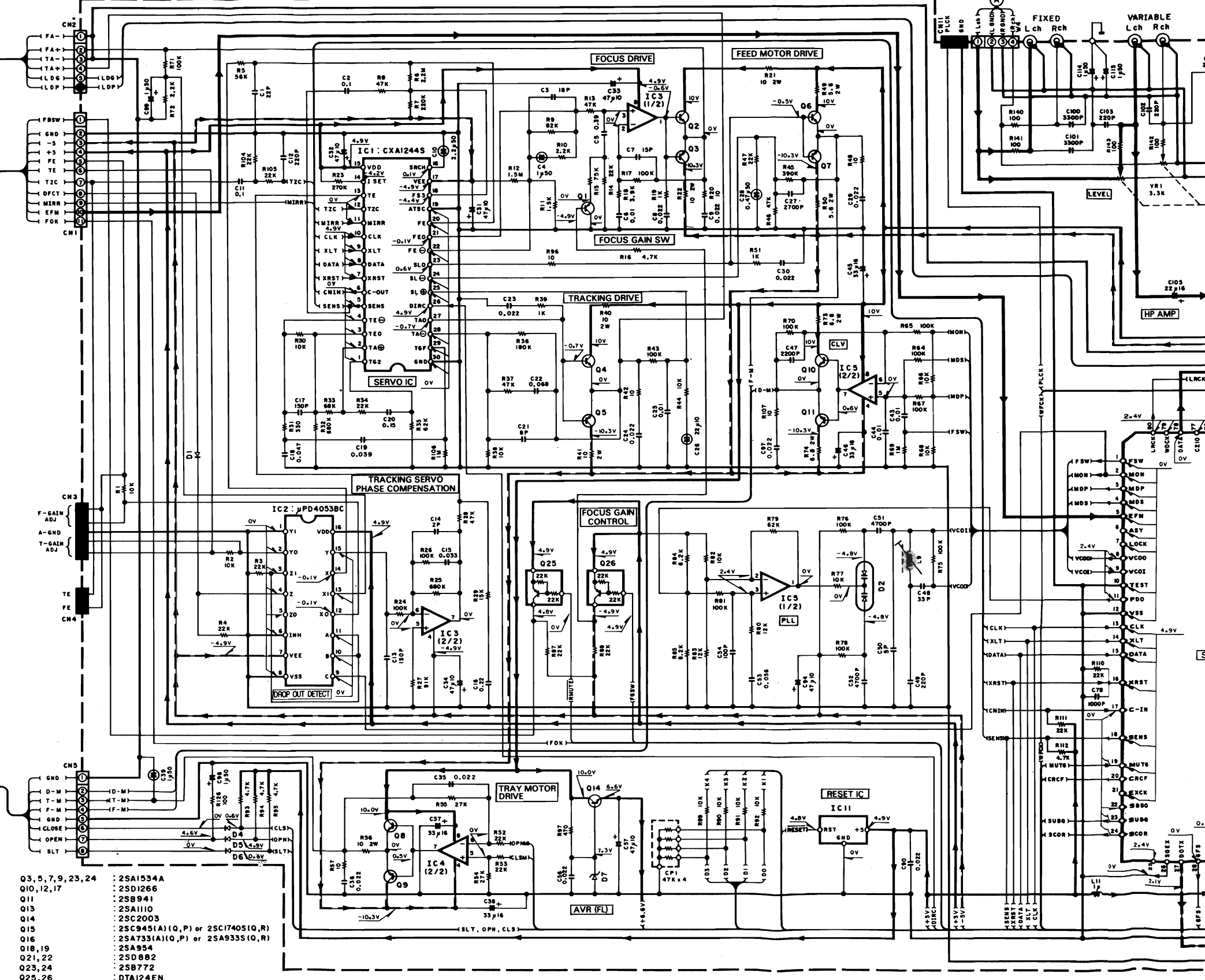
• Die angegebenen Gleichspannungswerte wurden mit einem hochohmigen Voltmeter gemessen. Dabei schwanken die Meßwerte aufgrund von Unterschieden zwischen einzelnen Instrumenten oder Geräten u. U. geringfügig.

- | | |
|--|--------------------------------|
| PCM56P-K | CXA1244S |
| DTA124EN | CXK5816SP-12L
CXK5816SP-15L |
| 2SA1534A
2SA733(A)
2SA954
2SA999
2SC2003
2SC2878
2SC3940A
2SC945(A) | CXA1081M |
| 2SA1110
2SB772
2SD882 | LB1294 |
| 2SD1266 | CXD1125OZ |
| DTC114YFF
DTC143EFF | TD62003AP
UPD4053BC |
| 2SA933B
2SC1740S | TC17G005AF-0048 |
| 2SB941 | UPD75216ACW-051 |
| NJM4558D
NJM5532D-D | SM5804D |
| | M5F78M05L
M5F78M06L |
| | M5218P-K
M5220P |
| | M5218L |
| | M51951ASL |
| | M5F79M05L
M5F79M06L |
| | TC74HC174F |
| | TC74HC00P
TC74HC08P |
| | LB1433N |

MECHANISM ASS'Y (X92-1210-00)

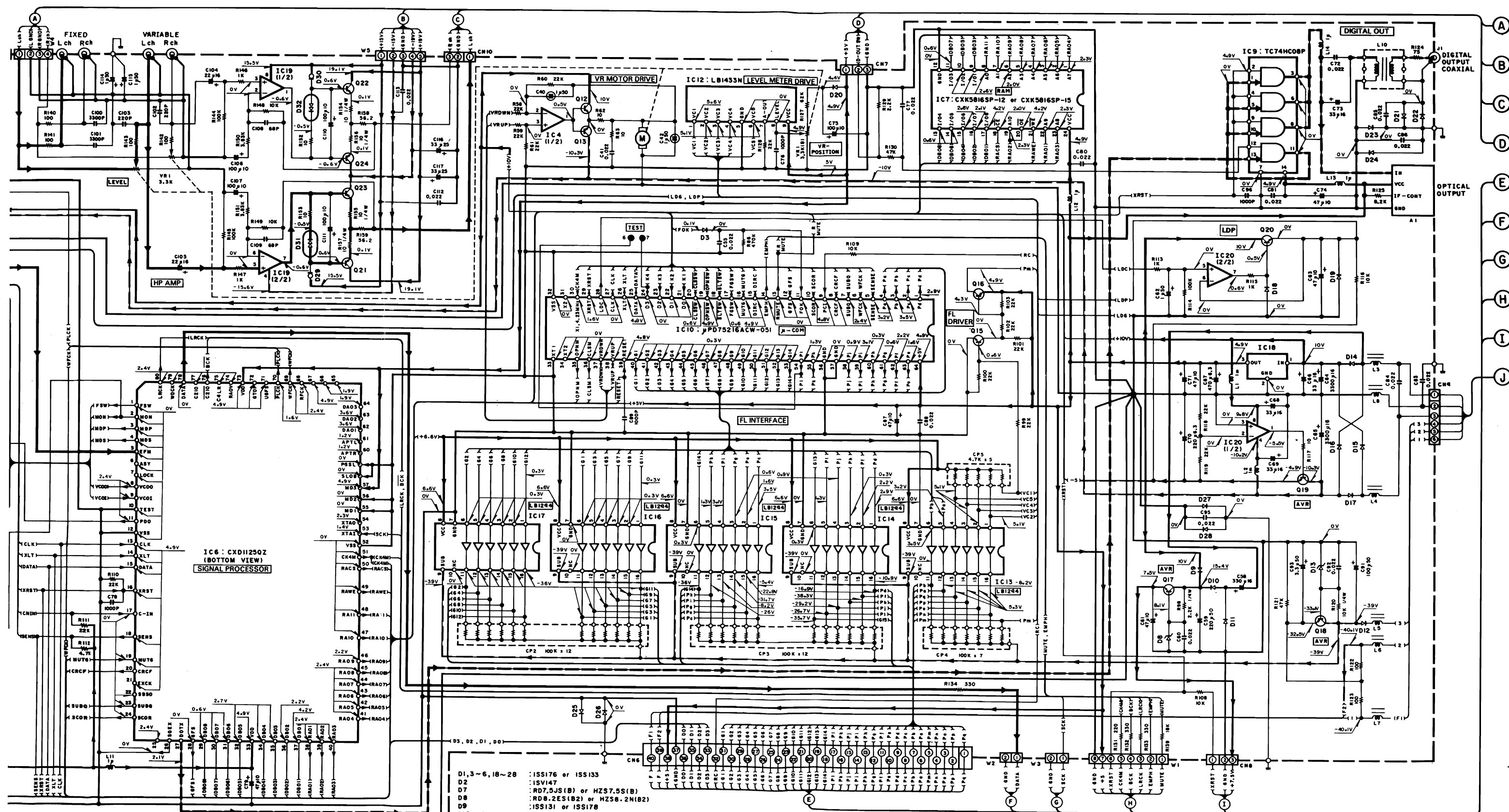


(X32-1170-00)



- (X32-1170-00)
- IC1 : CXA1244S
IC2 : μ PD4053BC
IC3,5 : M5218P-K
IC4,20 : NJM4558D
IC6 : CXD11250Z
IC7 : CXK5816SP-I2L or CXK5816SP-I5L
- IC9 : TC74HC08P
IC10 : μ PD75216ACW-051
IC11 : M5195IASL
IC12 : LB1433N
IC13-17 : LB1294
- IC18 : M5F78M05L
IC19 : M5218L
- Q1 : 2SC2878
Q2,4,6,8,20 : 2SC3940A
Q23,24 : 2SB772
Q25,26 : DTA124EN

- Q3,5,7,9,23,24 : 2SA1534A
Q10,12,17 : 2SD1266
Q11 : 2SB941
Q13 : 2SA1110
Q14 : 2SC2003
Q15 : 2SC945(A)(I,O,P) or 2SC1740S(I,O,R)
Q16 : 2SA733(A)(I,O,P) or 2SA933S(I,O,R)
Q18,19 : 2SA954
Q21,22 : 2SD882
Q23,24 : 2SB772
Q25,26 : DTA124EN



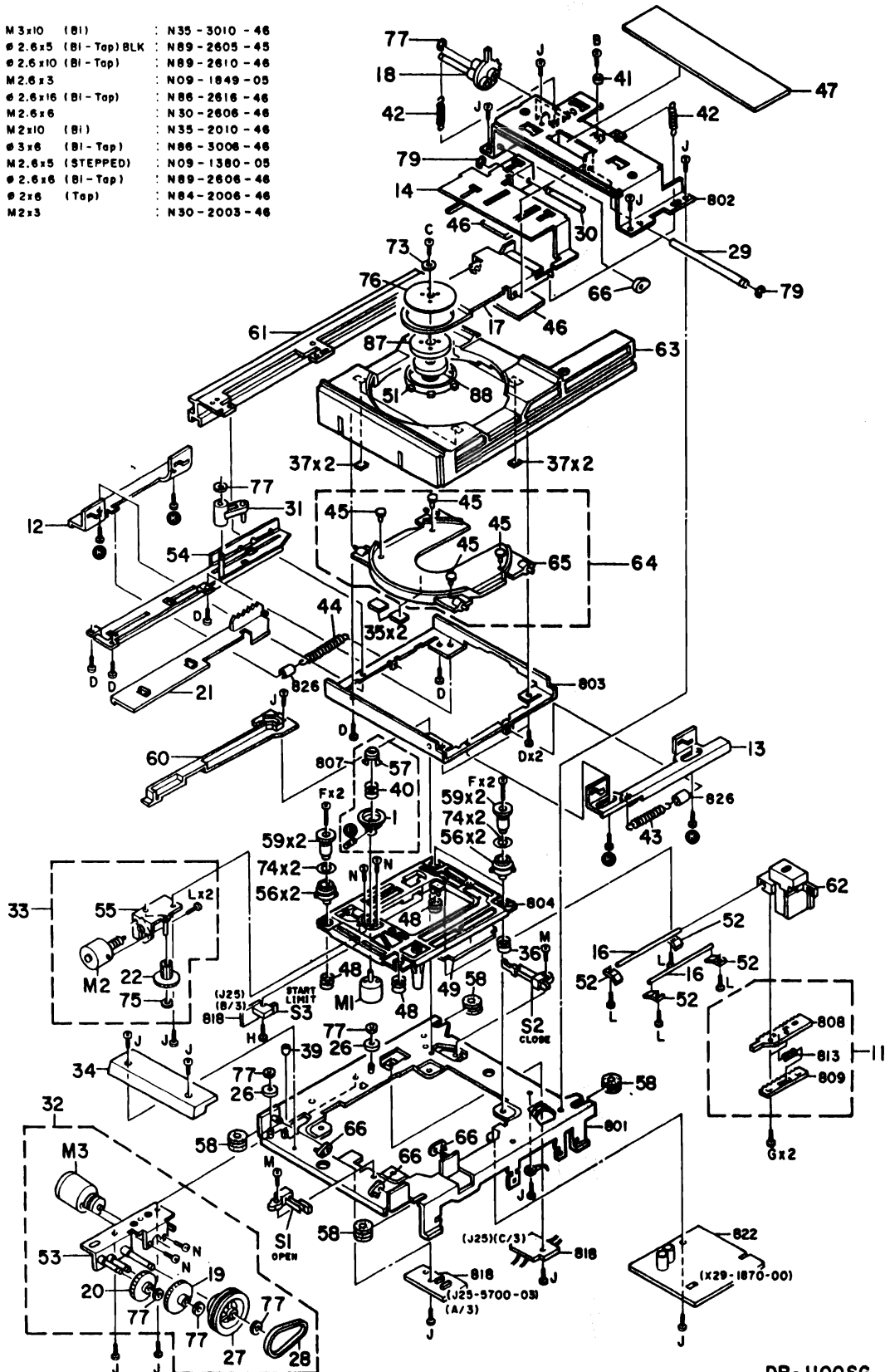
D1, 3 - 6, 18 - 28	: ISS176 or ISS133
D2	: ISV147
D7	: RD7.5S(B) or HZS7.5S(B)
D8	: RD8.2ES(B2) or HZS8.2N(B2)
D9	: ISS131 or ISS178
D10 ~ 12, 14 ~ 17	: DSM1A1
D13	: RD33JS (B)
D29, 30	: E - 272
D31, 32	: MA27W

CAUTION: For continued safety, replace safety critical components only with manufacturer's recommended parts (refer to parts list). **⚠** Indicates safety critical components. To reduce the risk of electric shock, leakage-current or resistance measurements shall be carried out (exposed parts are acceptably insulated from the supply circuit) before the appliance is returned to the customer.

- DC voltages are measured with a high impedance voltmeter. Values may vary slightly due to variations between individual instruments or/and units.
- Les tensions c.c. doivent être mesurées avec un voltmètre à haute impédance. Les valeurs peuvent différer légèrement du fait des variations inhérentes aux appareils et aux instruments de mesure individuels.
- Die angegebenen Gleichspannungswerte wurden mit einem hochohmigen Voltmeter gemessen. Dabei schwanken die Meßwerte aufgrund von Unterschieden zwischen einzelnen Instrumenten oder Geräten u. U. geringfügig.

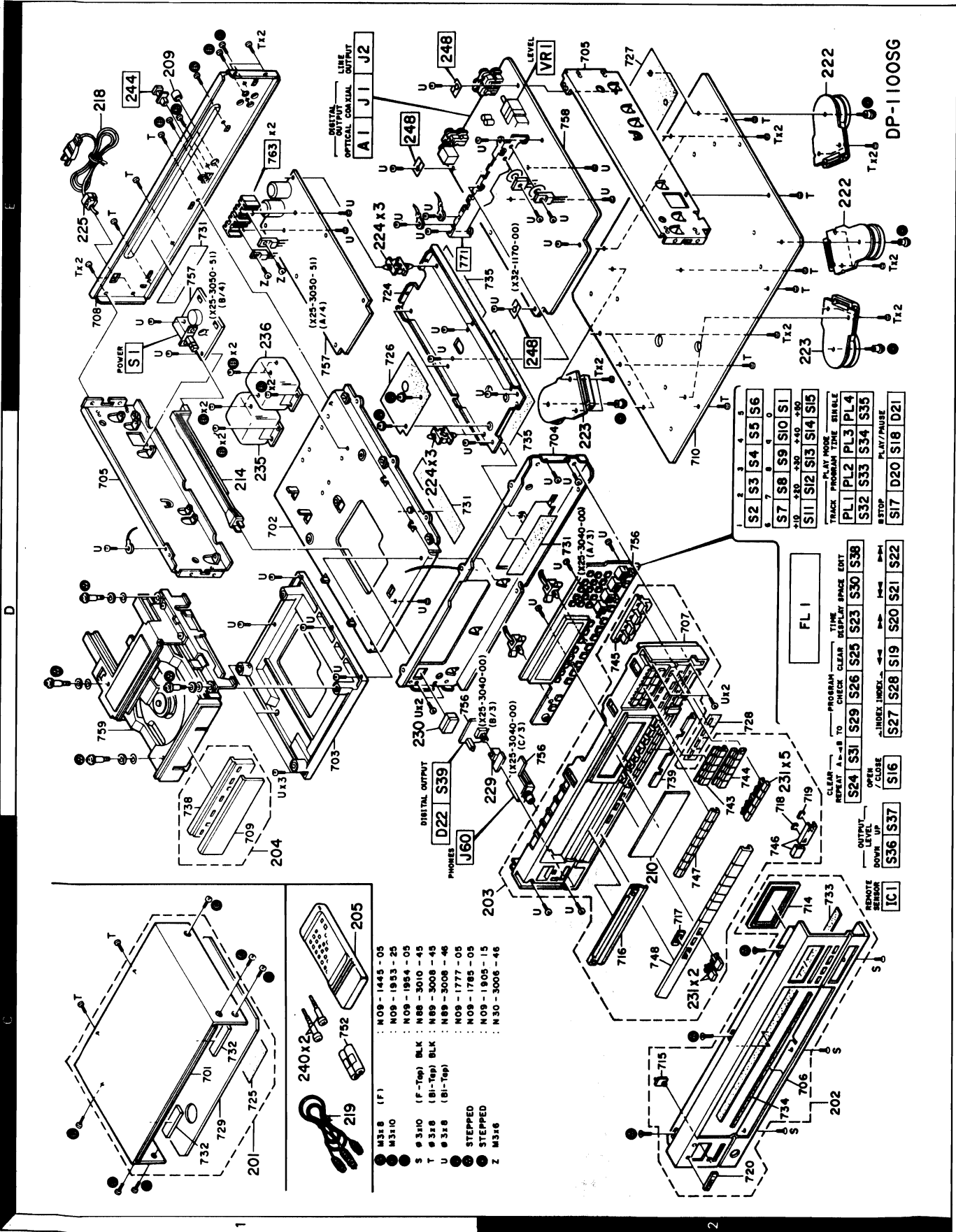
EXPLODED VIEW (MECHANISM)

- | | | | |
|---|----------------------|---|-------------|
| B | M 3x10 (Bl) | : | N35-3010-46 |
| C | # 2.6x5 (Bl-Tap) BLK | : | N89-2605-45 |
| D | # 2.6x10 (Bl-Tap) | : | N89-2610-46 |
| E | M 2.6x3 | : | N09-1849-05 |
| F | # 2.6x16 (Bl-Tap) | : | N86-2616-46 |
| G | M 2.6x6 | : | N30-2606-46 |
| H | M 2x10 (Bl) | : | N35-2010-46 |
| J | # 3x6 (Bl-Tap) | : | N86-3006-46 |
| K | M 2.6x5 (STEPPED) | : | N09-1380-05 |
| L | # 2.6x6 (Bl-Tap) | : | N89-2606-46 |
| M | # 2x6 (Tap) | : | N84-2006-46 |
| N | M 2x3 | : | N30-2003-46 |



DP-1100SG

EXPLODED VIEW (UNIT)



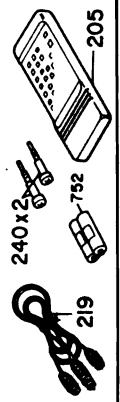
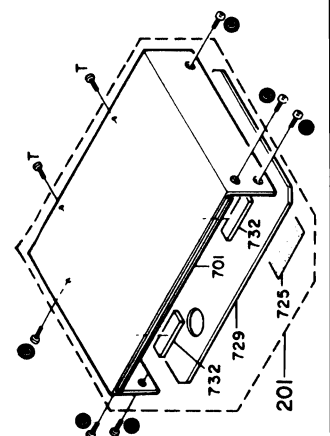
DP-1100SG

- M 318 (F)
- M 310
- S 310 (F-Top) BLK
- T 318 (B1-Top) BLK
- U 316 (B1-Top)
- M 09-1445-05
- N 09-1953-25
- N 09-1954-05
- N 88-3010-45
- N 89-3008-45
- N 88-3008-46
- N 09-1777-05
- N 09-1785-05
- N 09-1905-15
- N 30-3006-46
- STEPPED
- STEPPED
- M 316

S2	S3	S4	S5	S6
S7	S8	S9	S10	S1
S11	S12	S13	S14	S15

TRACK PLAY MODE SINGLE
 PL1 PL2 PL3 PL4
 S32 S33 S34 S35
 S202 PLAY/PAUSE
 S17 D20 S18 D21

FL 1
CLEAR A-B TO PROGRAM CHECK CLEAR DISPLAY SPACE EXT
S24 S31 S29 S26 S25 S23 S30 S38
OPEN / CLOSE INDEX INDEX
DOWN UP
S36 S37 S16
S27 S28 S19 S20 S21 S22



PARTS LIST

* New Parts

Parts without Parts No. are not supplied.

Les articles non mentionnés dans le Parts No. ne sont pas fournis.

Teile ohne Parts No. werden nicht geliefert.

Ref. No. 参照番号	Address 位置	New Parts 新	Parts No. 部品番号	Description 部品名/規格	Desti- nation 仕向	Re- marks 備考
DP-1100SG						
201	1C	*	A01-1618-12	METALLIC CABINET ASSY		
202	2C	*	A20-5343-02	PANEL ASSY		
203	2C	*	A22-0913-02	SUB PANEL		
204	1C	*	A29-0112-04	PANEL		
205	1C	*	A70-0160-05	REMOTE CONTROLLER ASSY		
209	1E	*	B09-0068-05	CAP (COAXIAL)		
210	2C	*	R10-0897-04	FRONT GLASS (DISPLAY)		
-	-	-	B46-0122-13	WARRANTY CARD	E	
-	-	-	B46-0143-03	WARRANTY CARD	T	
-	-	*	B50-8524-00	INSTRUCTION MANUAL (ENGLISH)		
-	-	*	B50-8525-00	INSTRUCTION MANUAL (FRENCH)	E	
-	-	*	B50-8527-00	INSTRUCTION MANUAL (G.D.I.)	E	
-	-	-	B58-0400-04	CAUTION CARD		
-	-	-	B58-0849-04	CAUTION CARD		
214	1D	*	D21-1395-03	EXTENSION SHAFT (POWER)		
△ △ 218	1E	*	E30-0459-05	AC POWER CORD	E	
218	1E	*	E30-1416-05	AC POWER CORD	T	
219	1C	*	E30-2293-05	AUDIO CORD		
-	-	*	H01-7660-04	ITEM CARTON CASE		
-	-	*	H10-3481-02	POLYSTYRENE FRAMED FIXTURE (L)		
-	-	*	H10-3482-02	POLYSTYRENE FRAMED FIXTURE (R)		
-	-	*	H10-3590-04	POLYSTYRENE FRAMED FIXTURE		
-	-	-	H21-0244-04	PROTECTION SHEET		
-	-	*	H25-0232-04	PROTECTION BAG (235X350XD.03)		
-	-	*	H25-0319-04	PROTECTION BAG		
222	2E	*	J02-0356-05	INSULATOR ASSY (R)		
223	2D, 2E	*	J02-0357-05	INSULATOR ASSY (L)		
224	1D, 1E	*	J19-2855-05	UNIT HOLDER		
△ 225	1E	*	J42-0083-05	POWER CORD BUSHING		
-	-	-	J61-0050-15	WIRE BAND		
-	-	-	J61-0070-05	WIRE BAND		
-	-	-	J61-0307-05	WIRE BAND		
229	2D	*	K27-1514-04	KNOB (BUTTON) DIGITAL OUTPUT		
230	1D	*	K29-2516-04	KNOB (BUTTON) POWER		
231	2C, 2D	*	K29-2648-04	KNOB (BUTTON) OUTPUT LEVEL +10		
△ 235	1D	*	L01-4722-05	POWER TRANSFORMER (230V)		
236	1E	*	L01-4732-05	POWER TRANSFORMER (230V)		
240	1C	*	N09-1906-05	STEPPED SCREW		
A	2C	*	N09-1445-05	SET SCREW (M3XR)		
R	1D, 1E	*	N09-1953-15	MACHINE SCREW (TRANS. REAR)		
C	1C	*	N09-1954-05	MACHINE SCREW (CASE)		
V	1D, 1E	*	N09-1777-05	SEMS (TAPTITE SCREW) SHEET		
W	1D	*	N09-1785-05	STEPPED SCREW (MECHA)		
Y	2D, 2E	*	N09-1905-15	STEPPED SCREW (FRONT)		
DISPLAY UNIT (X25-3040-00)						
D20	2D	*	R30-1010-05	LEFT SIDE OF DISPLAY		
D21 +22	1C, 2D	*	R30-1012-05	LEFT SIDE OF DISPLAY		
R11 -4	2D	*	R30-1207-05	LAMP (PLAY MODE)		
C1 +2	-	-	C01-0085-05	CERAMIC OSCILLATOR		

E: Scandinavia & Europe K: USA P: Canada

U: PX (Far East, Hawaii) T: England M: Other Areas

UE: AAFES (Europe) X: Australia

△ indicates safety critical components.

PARTS LIST

* New Parts

Parts without Parts No. are not supplied.

Les articles non mentionnés dans le Parts No. ne sont pas fournis.

Teile ohne Parts No. werden nicht geliefert.

Ref. No. 参照番号	Address 位置	New Parts 新	Parts No. 部品番号	Description 部品名/規格	Desti- nation 仕向	Re- marks 備考
C3 C4 .5			C91-0753-05 C91-0765-05	CHIP C 470PF K CERAMIC 0.0047UF M		
J60	1C		E11-0162-05	PHONE JACK (3P) PHONES		
CP1			R90-0498-05	MULTI-COMP 2.2KX4 J 1/8W		
S1 -38 S39	2D 1D		S40-1064-05 S40-2323-05	PUSH SWITCH PUSH SWITCH (DIGITAL OUTPUT)		
D1 -19 D1 -19			1SS131 1SS178	DIODE DIODE		
FL1 IC1 IC2	2D 1C		CP5322AGNR BX-1458 TC74HC174F	FLUORESCENT INDICATOR TUBE IC (REMOTE SENSOR) IC (D-FLIP FLOP)		
IC3			TD62003AP	IC (DARLINGTON DRIVER)		
D/A CONVERTER UNIT (X25-3050-51)						
244	1E		B09-0063-05	CAP		
C1 .2 C3 .4 C5 .6 C7 .8 C9 .10			C91-0980-05 C90-1334-05 C91-0175-05 CQ93HP2A203G CQ93HP2A332G	CERAMIC 15PF G NP-ELEC 47UF 10WV POLYSTY 56PF K MYLAR 0.020UF G MYLAR 3300PF G		
C11 -18 C19 .20 C21 .22 C25 .26 C29 -32		*	CK45FF1H103Z CQ93HP2A182G CE04KW1A101M CQ93HP2A242G CQ93HP2A242G	CERAMIC 0.010UF Z MYLAR 1800PF G ELECTRO 100UF 10WV MYLAR 2400PF G MYLAR 2400PF G		
C35 .36 C37 .38 C39 -42 C43 .44 C47 .48		*	CQ93HP2A242G CQ09FS1H151J CE04KW1C330M CE04KW0J471M CE04KW0J471M	MYLAR 2400PF G POLYSTY 150PF J ELECTRO 33UF 16WV ELECTRO 470UF 6.3WV ELECTRO 470UF 6.3WV		
C49 .50 C51 .52 C53 .54 C55 -57 C61 -68		*	CE04KW0J222M CQ93HP2A162G CQ09FS1H471J C91-0647-05 C91-0170-05	ELECTRO 2200UF 6.3WV MYLAR 1600PF G POLYSTY 470PF J CERAMIC 0.01UF P POLYSTY 22PF K		
C96 -99 C100-101 C102-105 C107 C108			CE04KW1C330M CE04KW1C332M CE04KW1C330M CE04KW1A470M CE04KW0J471M	ELECTRO 33UF 16WV ELECTRO 3300UF 16WV ELECTRO 33UF 16WV ELECTRO 47UF 10WV ELECTRO 470UF 6.3WV		
C110 C111,112 C113,114 C115 C120,121			CE04KW1A470M CE04KW0J222M C91-0769-05 CE04KW1H010M CE04KW1C330M	ELECTRO 47UF 10WV ELECTRO 2200UF 6.3WV CERAMIC 0.01UF M ELECTRO 1.0UF 50WV ELECTRO 33UF 16WV		
C122,123 C124,125 C126 C127,128 C129,130		*	CE04KW1E221M C90-1615-05 CE04KW1A101M CE04KW1E330M CE04KW1E222M	ELECTRO 220UF 25WV ELECTRO 3300UF 25WV ELECTRO 100UF 10WV ELECTRO 33UF 25WV ELECTRO 2200UF 25WV		
L1 -6 L7 -12			L40-1021-11 L33-0328-05	SMALL FIXED INDUCTOR (1.0MH,K) CHOKE COIL		

E: Scandinavia & Europe K: USA P: Canada
U: PX(Far East, Hawaii) T: England M: Other Areas
UE: AAFES(Europe) X: Australia

▲ indicates safety critical components.

PARTS LIST

* New Parts

Parts without Parts No. are not supplied.

Les articles non mentionnés dans le Parts No. ne sont pas fournis.

Teile ohne Parts No. werden nicht geliefert.

Ref. No. 参照番号	Address 位置	New Parts 新	Parts No. 部品番号	Description 部品名/規格	Desti- nation 仕向	Re- marks 備考
L13 L14 -22 L23 .24 X1			L79-0733-05 L40-1092-17 L40-1021-11 L77-1135-05	LINE FILTER SMALL FIXED INDUCTOR(1.0H,M) SMALL FIXED INDUCTOR(1.0MH,K) CRYSTAL RESONATOR		
R5 .6 R9 .10 R11 .12 R13 .14 R15 .16			RN14BK2C1001F RN14BK2C10R0F RN14BK2C1003F RN14BK2C1211F RN14BK2C8250F	RN 1.00K F 1/6W RN 10.0 F 1/6W RN 100K F 1/6W RN 1.21K F 1/6W RN 825.0 F 1/6W		
R19 .20 R27 .28 R37 .38 R39 .40 R47 .48			RN14BK2C1001F RN14BK2C1621F RN14BK2C9092F RN14BK2C1961F RN14BK2C6341F	RN 1.00K F 1/6W RN 1.62K F 1/6W RN 90.9K F 1/6W RN 1.96K F 1/6W RN 6.34K F 1/6W		
R49 .54 R55 .56 R57 .58 R59 .64 R65 .66			RN14BK2C3241F RN14BK2C9092F RN14BK2C1961F RN14BK2C3241F RN14BK2C1621F	RN 3.24K F 1/6W RN 90.9K F 1/6W RN 1.96K F 1/6W RN 3.24K F 1/6W RN 1.62K F 1/6W		
R69 .70 R71 .72 R75 -78 R79 -82 R83 .84			RN14BK2C1963F RN14BK2C9092F RN14BK2C6811F RN14BK2C1002F RN14BK2C1003F	RN 196K F 1/6W RN 90.9K F 1/6W RN 6.81K F 1/6W RN 10.0K F 1/6W RN 100K F 1/6W		
R85 .86 R89 .90 R95			RN14BK2C1002F RN14BK2C1001F RN14BK2C1004F	RN 10.0K F 1/6W RN 1.00K F 1/6W RN 1.00M F 1/6W		
VR1 .2 VR3 .4		*	R12-1100-05 R12-3147-05	TRIMMING PBT. (2.2K) DAC OUTPUT TRIMMING PBT. (47K) DAC		
VR5 .6		*	R12-1102-05	TRIMMING PBT. DAC		
K1 .2 S1	1E		S51-2074-05 S40-1103-05	MAGNETIC RELAY PUSH SWITCH (POWER TYPE)		
PH1			T95-0101-05	BPT8 ISOLATOR		
D1 -8 D9 D9 D10 -13 D10 -13			D5M1A1 HZ35.1S(B2) R05.1JS(B2) 1SS133 1SS176	DIODE ZENER DIODE ZENER DIODE DIODE DIODE		
D14 D14 D15 .16 D15 .16 D17		*	HZ511N(B2) RD11FS(B2) HZ520S(B2) RD20JS(B2) E-102	ZENER DIODE ZENER DIODE ZENER DIODE ZENER DIODE CONSTANT CURRENT DIODE		
D18 -21 D18 -21 IC1 .2 IC3 -10 IC13			1SS133 1SS176 PCM56P-K NUM5532D-D MS220P	DIODE DIODE IC (DA CONVERTER) IC (8P AMP X2) IC (8P AMP X2)		
IC14 IC15 IC16 IC17 IC22			SMS804D TC176005AF-0048 MSF79M6L MSF79M6L MSF79M05H	IC (DIGITAL FILTER) IC (VCR) IC (VOLTAGE REGULATOR / +5V) IC (VOLTAGE REGULATOR / +5V) IC (VOLTAGE REGULATOR / +5V)		

E: Scandinavia & Europe K: USA P: Canada
U: PX(Far East, Hawaii) T: England M: Other Areas
UE: AAFES(Europe) X: Australia

▲ indicates safety critical components.

PARTS LIST

* New Parts

Parts without Parts No. are not supplied.

Les articles non mentionnés dans le Parts No. ne sont pas fournis.

Teile ohne Parts No. werden nicht geliefert.

Ref. No. 参照番号	Address 位置	New Parts 新	Parts No. 部品番号	Description 部品名/規格	Desti- nation 仕	Re- marks 備考
IC23 IC24 Q2 Q3 Q10 .11		*	M5F78M05L M51951A9L 2SD1266(P) 2SB941(P) DTC114YFF	IC(VOLTAGE REGULATOR/ +5V) IC(SYSTEM RESET) TRANSISTOR TRANSISTOR DIGITAL TRANSISTOR		
Q12 .13 Q14 Q14		*	DTC143EFF 2SA733(A)(D,P) 2SA999(E,F)	DIGITAL TRANSISTOR TRANSISTOR TRANSISTOR		
CONTROL CIRCUIT UNIT (X29-1870-00)						
Q1 Q2 Q3 Q4 Q5			CE04KW0J331M CE04KW1A470M CE04KW1HR47M CE04KW1A470M CF92FV1H333J	ELECTRO 330UF 6.3WV ELECTRO 47UF 10WV ELECTRO 0.47UF 50WV ELECTRO 47UF 10WV MF 0.033UF J		
Q6 Q7 Q8 Q9 Q11	.10		CF92FV1H102J CF92FV1H104J CK45FF1H103Z C91-0725-05 CF92FV1H222J	MF 1000PF J MF 0.10UF J CERAMIC 0.010UF Z CERAMIC 15PF J MF 2200PF J		
Q13 Q14			CE04KW0J331M C91-0700-05	ELECTRO 330UF 6.3WV CERAMIC 0.1UF J		
VR1 .2 VR3 .4		*	R12-3071-05 R12-3072-05	TRIMMING PBT. (10K)FB/TR GAIN TRIMMING PBT. (FB/TR ERROR)		
IC1 IC2 Q1		*	CXA1081M TC74HC00P 2SC287B	IC(RF AMP) IC(DUAD 2-INPUT NAND GATE) TRANSISTOR		
CD PLAYER UNIT (X32-1170-00)						
Q1 Q2 Q3 Q4 Q5			C91-0729-05 CF92FV1H104J CC45FSL1H180J C90-1349-05 CF92FV1H394J	CERAMIC 22PF J MF 0.10UF J CERAMIC 18PF J NP-ELEC 1UF 50WV MF 0.39UF J		
Q6 Q7 Q8 Q9 Q10			CF92FV1H103J CC45FSL1H150J CK45FF1H223Z C91-0085-05 C90-1350-05	MF 0.010UF J CERAMIC 15PF J CERAMIC 0.022UF Z CERAMIC 0.022UF N NP-ELEC 2.2UF 50WV		
Q11 Q12 Q13 Q14 Q15			CF92FV1H104J C91-0749-05 CC45FSL1H151J CC45FSL1H020C CF92FV1H683J	MF 0.10UF J CERAMIC 220PF K CERAMIC 150PF J CERAMIC 2.0PF C MF 0.068UF J		
Q16 Q17 Q18 Q19 Q20			CF92FV1H474J CC45FSL1H151J CF92FV1H473J CF92FV1H393J CF92FV1H154J	MF 0.47UF J CERAMIC 150PF J MF 0.047UF J MF 0.039UF J MF 0.15UF J		
Q21 Q22 Q23 Q24 Q25			CC45FSL1H080D CF92FV1H154J CK45FF1H223Z C91-0085-05 CF92FV1H103J	CERAMIC 8.0PF D MF 0.15UF J CERAMIC 0.022UF Z CERAMIC 0.022UF N MF 0.010UF J		
Q26			C90-1333-05	NP-ELEC 22UF 10WV		

E: Scandinavia & Europe K: USA P: Canada

U: PX(Far East, Hawaii) T: England M: Other Areas

UE: AAFES(Europe) X: Australia

△ indicates safety critical components.

PARTS LIST

* New Parts

Parts without Parts No. are not supplied.

Les articles non mentionnés dans le Parts No. ne sont pas fournis.

Teile ohne Parts No. werden nicht geliefert.

Ref. No. 参照番号	Address 位置	New Parts 新	Parts No. 部品番号	Description 部品名/規格	Desti- nation 仕	Re- marks 備考
C27 C28 C29 C30 C31 -34			CF92FV1H272J C90-1331-05 CK45FF1H223Z C91-0085-05 CE04KW1A470M	MF 2700PF J NP-ELEC 0.47UF 50WV CERAMIC 0.022UF Z CERAMIC 0.022UF N ELECTRO 47UF 10WV		
C35 C36 C37 .38 C39 .40 C41			CK45FF1H223Z C91-0085-05 CE04KW1C330M C90-1349-05 C91-0085-05	CERAMIC 0.022UF Z CERAMIC 0.022UF N ELECTRO 33UF 16WV NP-ELEC 1UF 50WV CERAMIC 0.022UF N		
C42 C43 .44 C45 .46 C47 C48			C90-1349-05 CF92FV1H103J CE04KW1C330M CF92FV1H222J CC45FUJ1H330J	NP-ELEC 1UF 50WV MF 0.010UF J ELECTRO 33UF 16WV MF 2200PF J CERAMIC 33PF J		
C49 C50 C51 .52 C53 C54			CC45FSL1H221J CC45FUJ1H050C CF92FV1H472J CF92FV1H563J CC45FSL1H101J	CERAMIC 220PF J CERAMIC 5.0PF C MF 4700PF J MF 0.056UF J CERAMIC 100PF J		
C55 C56 C57 C58 C59			CF92FV1H223J CK45FF1H223Z CE04KW1A470M CE04KW1C331M CE04KW1H221M	MF 0.022UF J CERAMIC 0.022UF Z ELECTRO 47UF 10WV ELECTRO 330UF 16WV ELECTRO 220UF 50WV		
C60 C61 C62 C63 C64 .65			CK45FF1H223Z CE04KW1A470M CE04KW1H010M CE04KW1A470M CE04KW1C332M	CERAMIC 0.022UF Z ELECTRO 47UF 10WV ELECTRO 1.0UF 50WV ELECTRO 47UF 10WV ELECTRO 3300UF 16WV		
C66 C67 C68 .69 C70 C71			CE04KW1C330M CE04KW0J471M CE04KW1C330M CE04KW0J221M CE04KW1A470M	ELECTRO 33UF 16WV ELECTRO 470UF 6.3WV ELECTRO 33UF 16WV ELECTRO 220UF 6.3WV ELECTRO 47UF 10WV		
C72 C73 C74 C75 C76			CK45FF1H223Z CE04KW1C330M CE04KW1A470M CE04KW1A101M C91-0757-05	CERAMIC 0.022UF Z ELECTRO 33UF 16WV ELECTRO 47UF 10WV ELECTRO 100UF 10WV CERAMIC 0.001UF K		
C77 C78 C79 C80 C81			CK45FF1H223Z C91-0757-05 CE04KW1A470M CK45FF1H223Z C91-0085-05	CERAMIC 0.022UF Z CERAMIC 0.001UF K ELECTRO 47UF 10WV CERAMIC 0.022UF Z CERAMIC 0.022UF N		
C82 -86 C87 C88 C89 C90			CK45FF1H223Z CE04KW1A470M C91-0085-05 CK45FB1H102K CK45FF1H223Z	CERAMIC 0.022UF Z ELECTRO 47UF 10WV CERAMIC 0.022UF N CERAMIC 1000PF K CERAMIC 0.022UF Z		
C91 C92 C93 C94 C95			CE04KW1H101M CK45FF1H223Z CE04KW1H3R3M CE04KW1A470M C91-0085-05	ELECTRO 100UF 50WV CERAMIC 0.022UF Z ELECTRO 3.3UF 50WV ELECTRO 47UF 10WV CERAMIC 0.022UF N		

E: Scandinavia & Europe K: USA P: Canada

U: PX(Far East, Hawaii) T: England M: Other Areas

UE: AAFES(Europe) X: Australia

△ indicates safety critical components.

PARTS LIST

× New Parts
 Parts without Parts No. are not supplied.
 Les articles non mentionnés dans le Parts No. ne sont pas fournis.
 Teile ohne Parts No. werden nicht geliefert.

Ref. No. 参照番号	Address 位置	New Parts 新	Parts No. 部品番号	Description 部品名/規格	Desti- nation 仕向	Re- marks 備考
C96 C97 C98 C99 C100-101			C91-0757-05 Ck45FF1H2232 CE04KW1H010M CE04KW1H010M CF92FV1H032J	CERAMIC 0.001UF K CERAMIC 0.022UF J ELECTRN 1.0UF 50WV ELECTRN 1.0UF 50WV MF 3300PF J		
C102-103 C104-105 C106-107 C108-109 C110-111			CC45FSL1H221J CE04KW1C230M CE04KW1A101M CC45FSL1H468J CE04KW1A101M	CERAMIC 220PF J ELECTRN 22UF 16V ELECTRN 100UF 10WV CERAMIC 68PF J ELECTRN 100UF 10WV		
C112-113 C114 C115 C116-117			C91-0085-05 CE04KW1H010M CE04KW1H010M CE04KW1E330M	CERAMIC 0.022UF N ELECTRN 1.0UF 50WV ELECTRN 1.0UF 50WV ELECTRN 33UF 25WV		
248 J1 J2	1E+2E 1E 1E	*	E23-0149-05 E13-0131-05 E13-0485-05	TERMINAL PHONE JACK (DIGITAL OUTPUT) PHONE JACK (LINE OUTPUT)		
L1 +2 L3 -8 L9 L10 L11 -13 L14			L40-1021-14 L33-0323-05 L32-0328-15 L39-0155-05 L40-1092-17 L40-1092-17	SMALL FIXED INDUCTOR(1.0MH+K) CHOKE COIL OSCILLATING COIL MATCHING COIL SMALL FIXED INDUCTOR(1UH+M) SMALL FIXED INDUCTOR(1UH+M)		
CP1 CP2 +3 CP4 CP5 R21 +22			R90-0202-05 R90-0272-05 R90-0278-05 R90-0453-05 RS14DB3D100J	MULTI-COMP 47KX4 J 1/6W MULTI-COMP 100KX12 J 1/6W MULTI-COMP 100KX7 J 1/6W MULTI-COMP 4.7K J 1/6W FL-PROOF RS 10 J 2W		
R40 +41 R49 +50 R56 R62 R73 +74			RS14DB3D100J RS14DB3D5R6J RS14DB3D100J RS14DB3D100J RS14DB3D6R8J	FL-PROOF RS 10 J 2W FL-PROOF RS 5.6 J 2W FL-PROOF RS 10 J 2W FL-PROOF RS 10 J 2W FL-PROOF RS 6.8 J 2W		
R140-143 R144-145 R146-147 R148-149 R150-151			RN14BK2C1000F RN14BK2C1003F RN14BK2C1001F RN 10.0K F 1/6W RN14BK2C1002F RN 3.03K F 1/6W	RN 100.0 F 1/6W RN 100K F 1/6W RN 1.00K F 1/6W RN 10.0K F 1/6W RN 3.03K F 1/6W		
R152-153 R154-157 R158-159 VR1			RN14BK2C10R0F RN14BK2E10R0F RN14BK2E56R2F R29-1002-05	RN 10.0 F 1/6W RN 10.0 F 1/4W RN 56.2 F 1/4W POTENTIOMETER(3K B)LEVEL		
D1 D1 D2 D3 +6 D3 +6			1S5133 1S5176 1S5147 1S5133 1S5176	DIODE DIODE VARISTOR DIODE DIODE		
D7 D7 D8 D8 D9 D9			HZ57.5S(B) RD7.5J3(B) HZ58.2N(B2) RDB.2ES(B2) 1S5131 1S5178	ZENER DIODE ZENER DIODE ZENER DIODE ZENER DIODE DIODE DIODE		

E: Scandinavia & Europe K: USA P: Canada
 U: PX(Far East, Hawaii) T: England M: Other Areas
 UE: AAFES(Europe) X: Australia

△ indicates safety critical components.

PARTS LIST

× New Parts
 Parts without Parts No. are not supplied.
 Les articles non mentionnés dans le Parts No. ne sont pas fournis.
 Teile ohne Parts No. werden nicht geliefert.

Ref. No. 参照番号	Address 位置	New Parts 新	Parts No. 部品番号	Description 部品名/規格	Desti- nation 仕向	Re- marks 備考
D10 -12 D13 D14 -17 D18 -28 D18 -28		*	DSM1A1 RD33J5(B) DSM1A1 1S5133 1S5176	DIODE ZENER DIODE DIODE DIODE DIODE		
D29 +30 D31 +32 D33 D33 IC1			E-272 7A27W 1S5133 1S5176 CXA1244S	CONSTANT CURRENT DIODE VARISTOR DIODE DIODE IC(SERVO SIGNAL PROCESSOR)		
IC2 IC3 IC4 IC5 IC6			JPD4053BC MS218P-K NJM4558D MS218P-K CXD11250Z	IC(3-INPUT 2CH MPX/DE-MPX) IC(OP AMP X2) IC(OP AMP X2) IC(OP AMP X2) IC(DIGITAL SIGNAL PROCESSOR)		
IC7 IC7 IC9 IC10 IC11			CXK5816SP-12L CXK5816SP-15L TC74HC09P UPD75216ACW-051 MS1951ASL	IC(2KXB RAM) IC(2KXB RAM) IC(AND X2) IC(MICROPROCESSOR) IC(SYSTEM RESET)		
IC12 IC13-17 IC18 IC19 IC20		*	LB1433N LB1294 MSF78M05L MS218L NJM4558D	IC(LEVEL METER DRIVER) IC(6CH DARLINGTON DRIVER) IC(VOLTAGE REGULATOR/ +5V) IC(OP AMP X2) IC(OP AMP X2)		
Q1 Q2 Q3 Q4 Q5			2SC287B 2SC3940A 2SA1534A 2SC3940A 2SA1534A	TRANSISTOR TRANSISTOR TRANSISTOR TRANSISTOR TRANSISTOR		
Q6 Q7 Q8 Q9 Q10			2SC3940A 2SA1534A 2SC3940A 2SA1534A 2SD1266	TRANSISTOR TRANSISTOR TRANSISTOR TRANSISTOR TRANSISTOR		
Q11 Q12 Q13 Q14 Q15			2SB941 2SD1266 2SA1110 2SC2003 2SC1740S(D,R)	TRANSISTOR TRANSISTOR TRANSISTOR TRANSISTOR TRANSISTOR		
Q15 Q16 Q16 Q17 Q18 +19			2SC945(A)(D,P) 2SA733(A)(D,P) 2SA933S(D,R) 2SD1266 2SA954	TRANSISTOR TRANSISTOR TRANSISTOR TRANSISTOR TRANSISTOR		
Q20 Q21 +22 Q23 +24 Q25 +26			2SC3940A 2SD882 2SB772 DTA124EN	TRANSISTOR TRANSISTOR TRANSISTOR DIGITAL TRANSISTOR		
A1	1E		WD2-0784-05	ELECTRIC CIRCUIT MODULE		
MECHANISM ASS'Y (X92-1210-00)						
C1 C2 3			C90-1349-05 C91-0085-05	NP-ELET 1UF 50WV CERAMIC 0.022UF N		

E: Scandinavia & Europe K: USA P: Canada
 U: PX(Far East, Hawaii) T: England M: Other Areas
 UE: AAFES(Europe) X: Australia

△ indicates safety critical components.

PARTS LIST

* New Parts

Parts without Parts No. are not supplied.

Les articles non mentionnés dans le Parts No. ne sont pas fournis.

Teile ohne Parts No. werden nicht geliefert.

Ref. No. 参照番号	Address 位置	New Parts 新	Parts No. 部品番号	Description 部品名/規格	Desti- nation 仕向	Re- marks 備考
1	2A	*	D02-0073-04	TURNTABLE PLATTER		
11	3B	*	D13-0657-05	GEAR ASSY		
12	2A	*	D10-1266-03	SLIDER (L)		
13	2B	*	D10-1267-03	SLIDER (R)		
14	1A	*	D10-1268-03	SLIDER		
16	3B	*	D10-2011-04	ROD		
17	1B	*	D10-1271-03	ARM (CLAMPER)		
18	1A	*	D12-0105-15	LAM		
19	3A	*	D13-0157-08	GEAR		
20	3A	*	D13-0160-08	GEAR		
21	2A	*	D13-0161-03	GEAR		
22	3A	*	D13-0640-08	GEAR		
23	3A	*	D14-0162-04	ROLLER		
26	3A	*	D15-0220-08	PULLEY		
27	3A	*	D16-0169-08	BELT		
28	3A	*	D16-0169-08	BELT		
29	1B	*	D21-1051-04	SHAFT		
30	1B	*	D21-1052-04	SHAFT		
31	2A	*	D32-0122-04	STOPPER		
32	3A	*	D40-0583-05	DRIVE MECHANISM ASSY(LADING)		
33	2A	*	D40-0582-05	DRIVE MECHANISM ASSY(FEED)		
34	3A	*	F07-0503-04	COVER		
35	2A	*	G16-0160-04	SHEET		
36	3B	*	G01-1924-04	COMPRESSION SPRING(TRAY)		
37	2A,2B	*	G11-1238-04	CUSHION		
39	3A	*	G13-0189-04	CUSHION (CHASSIS)		
40	2A	*	G01-2105-04	COMPRESSION SPRING(TURNTABLE)		
41	1B	*	G01-0675-04	COMPRESSION SPRING		
42	1A,1B	*	G01-2102-04	EXTENSION SPRING		
43	2B	*	G01-1524-04	EXTENSION SPRING(FRONT-L)		
44	2A	*	G01-1525-04	EXTENSION SPRING		
45	2A,2B	*	G13-0166-04	CUSHION (TRAY)		
46	1B	*	G16-0117-04	SHEET (38X38X2)		
47	1B	*	G16-0134-04	SHEET (38X152X1)		
48	2A,3A	*	G01-1925-04	COMPRESSION SPRING		
49	3A	*	G16-0162-04	SHEET (LR DAMPER)		
51	1A	*	J11-0104-03	CLAMPER		
52	2B,3B	*	J21-5092-04	MOUNTING HARDWARE		
53	3A	*	J21-5098-08	MOUNTING HARDWARE ASSY		
54	2A	*	J21-3509-03	MOUNTING HARDWARE ASSY		
55	2A	*	J21-5097-08	MOUNTING HARDWARE ASSY		
56	2A,2B	*	J02-0192-05	INSULATOR		
57	2A	*	J19-2874-04	HOLDER (TURNTABLE)		
58	3A,3B	*	J42-0142-04	BUSHING (CHASSIS)		
59	2A,2B	*	J31-0282-04	COLLAR		
60	2A	*	J90-0143-03	GUIDE (STOPPER)		
61	1A	*	J90-0157-03	RAIL		
62	2B	*	J91-0341-05	PICKUP		
63	1B	*	J99-0024-12	TRAY		
64	2B	*	J99-0025-13	TRAY		
65	2B	*	J99-0026-13	TRAY		
66	3A,1B	*	J19-2875-14	HOLDER		
		*	J61-0307-05	WIRE BAND		
73	1A	*	N15-1026-45	FLAT WASHER (Ø2.6)		

E: Scandinavia & Europe K: USA P: Canada
 U: PX(Far East, Hawaii) T: England M: Other Areas
 UE: AAFES(Europe) X: Australia

▲ indicates safety critical components.

PARTS LIST

* New Parts

Parts without Parts No. are not supplied.

Les articles non mentionnés dans le Parts No. ne sont pas fournis.

Teile ohne Parts No. werden nicht geliefert.

Ref. No. 参照番号	Address 位置	New Parts 新	Parts No. 部品番号	Description 部品名/規格	Desti- nation 仕向	Re- marks 備考
74	2A,2B	*	N19-1072-04	FLAT WASHER		
75	3A	*	N19-0366-04	FLAT WASHER (Ø2.1)		
76	1A	*	N19-0945-04	FLAT WASHER (YØKE)		
77	1A,3A	*	N19-0891-04	FLAT WASHER (CHASSIS)		
79	1A,1B	*	N29-0207-04	RETAINING RING (Ø2.5)		
E	2A	*	N09-1849-05	SET SCREW (M2.6X3)TURNTABLE		
K	2A,2B	*	N09-1380-05	STEPPED SCREW (M2.6X5)		
51	2	*	S46-1045-05	LEAF SWITCH (OPEN/CLOSE)		
53	3A	*	S40-1101-05	PUSH SWITCH (START LIMIT)		
87	1A	*	T50-1036-04	YØKE		
88	1B	*	T99-0222-05	MAGNET		
M1	2A	*	T42-0439-05	DC MOTOR (DISC)		
M2	2A	*	T42-0437-08	MOTOR ASSY (FEED)		
M3	3A	*	T42-0438-08	MOTOR ASSY (LOADING)		

E: Scandinavia & Europe K: USA P: Canada
 U: PX(Far East, Hawaii) T: England M: Other Areas
 UE: AAFES(Europe) X: Australia

▲ indicates safety critical components.

